Optimal Design of Grid-Connected Voltage Source Converters Considering Cost and Operating Factors

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***Abstract*—This paper assesses the feasibility of three-phase pulse-width modulated (PWM) three-level voltage source converters (VSC), namely neutral-point-clamped (3L-NPC) and T-type (3L-T) as alternatives to two-level converter (2L-VSC) for low-voltage multi-MW renewable energy grid-connected converter applications. For this purpose, a novel design algorithm that takes switching frequency, capacity factor, modulation index, PWM scheme(s) and converter topology(ies) as input is unveiled to provide the design steps and performance benchmark for the specified topologies and modulation methods. Design of the *LCL*-filter is also addressed and equivalent output ripple performance criteria is used to benchmark the converter performances for a set of selected filter parameters. Main contribution of this algorithm is that it covers cost and operating factors of the design during the hardware design phase by introducing/modifying the terms of total cost of ownership (TCO) and return on investment time (ROI) considering the major energy markets. The design is detailed for 1 MVA system, and the results are summarized for 0.5 and 2 MVA systems. The study shows that 3L topologies perform more efficiently than 2L-VSC (T-type being the most prominent—with the shortest ROI) whereas the difference becomes much more prominent at the multi-MW range, provided that all three yield equivalent outputs fulfilling the stringent grid codes.**

***Index Terms*—Capacity factor, design, grid codes, inverter, *LCL*-filter, power harmonic filters, ROI, TCO, three-level converter, two-level converter, wind power generation.**

I. Introduction

THREE-PHASE grid-connected pulse-width modulated (PWM) voltage source converters (VSCs) have been increasingly utilized in renewable energy applications around the world. Photovoltaic (PV) applications (of solar farms, involving central inverters) are effective for the power ranges typically between 100 kW and 1 MW, whereas; wind energy applications (of individual turbines and/or on/offshore wind farms) involve 500 kW-7 MW power scale currently.

The insulated gate bipolar transistor (IGBT) based two-level VSC topology has been the standard industry solution to meet the requirements of the renewable energy applications due to its simplicity and low cost. Alternative solutions have difficulties to gain market share due to their increased complexity and cost. Prospective energy savings achieved with a different converter topology can only convince the customer if the initial costs are not too high and the investment yields a good return (Fig. 1). Yet, mainly for low-voltage multi-megawatt (multi-MW) applications, design limits of two-level VSC (2L-VSC) are reached due to the restricted technology of power semiconductors that can be switched up to only a few kHz for an acceptable efficiency. Hence, utilization of three or higher level based low-voltage converters becomes a technologically attractive solution beyond a certain power range.

In this paper, the standard 2L-VSC along with two other well-known 3L-VSC topologies, namely three-level neutral-point-clamped converter (3L-NPC) and three-level T-type converter (3L-T) are considered. In the literature, a great amount of publications contain benchmark studies between the 2L-VSC and the 3L-NPC/3L-T in terms of cost, performance, size and maintenance. In [1]-[7], an extensive analysis of the 2L-VSC design was provided. In [8]-[10], the 3L-T was examined in comparison with the 2L-VSC and the 3L-NPC in terms of efficiency and cost. However, these articles still do not provide concrete information regarding the existence of a power level/region where the 2L-VSC becomes less competitive against the 3L-VSC in low-voltage applications. Thereby, the primary motivation of this paper is to highlight the feasibility of the 2L, the 3L-NPC, and the 3L-T topologies regarding the system specifications. However, the optimal design of a grid-connected VSC cannot be confined only to the determination of the optimal topology, hence additional factors must be considered.

Conventional converter design methods are often developed based on rated operating point. Besides, designer's experience and/or widely accepted norms often decide upon the selection of switching frequency, hardware components and so on. Also, examination of return on investment time (ROI), i.e. pay-off time of the overall expenses is performed after on-site performance analysis is done (not during the design phase), which might lead to designs far from the optimal case. Yet, a single operating point approach does not hold for renewable energy applications due to intermittency since the input supplied to converter is not always rated and fluctuates tremendously. Thus, the mean penetration of the input power to the grid (capacity factor C.F for wind turbines, irradiation factor for PV, etc.) must be taken into account right in the design phase, including the total cost of ownership TCO (i.e. economic value of a plant over a determined lifetime) and the ROI. Fig. 1 conceptually illustrates other important parameters for an optimized converter design where the operational efficiency and the ROI are the main performance indicators.

All the design parameters of concern are shown with their interdependency. Selected VSC topology and modulation

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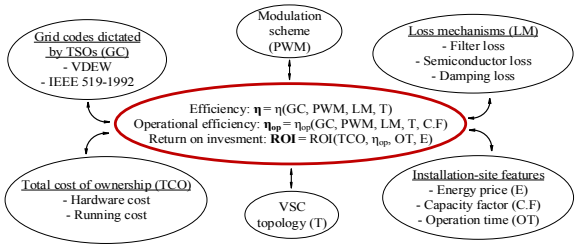


Fig. 1. Conceptual VSC design diagram depicting the interdependency of design parameters.

scheme together with loss mechanisms (semiconductor, filter and damping loss models being unveiled explicitly in the corresponding sections) and grid codes (dictated by transmission system operators, TSO) have a role on the overall efficiency of the system. Intermittency of the renewable energy is reflected via C.F definition (see Fig. 1). Hence, as a figure of merit, *operational efficiency* η_{op} is introduced and is used together with the hardware & running costs (TCO) and installation-site features (e.g. energy price where the plant is installed and operation time of the plant) for calculation of the ROI. Thus, once the candidate VSC topologies and PWM methods are nominated for a specific application, η_{op} and ROI are obtained at the end of the design phase, enabling to compare topologies (under the chosen PWM method) only regarding ROI where the shortest ROI addresses the optimal solution. Hence, a thorough design method is provided where C.F, ROI, and grid codes are parts of the design phase to unveil the fact that potential energy savings achieved with a different converter topology, PWM scheme, etc. might convince the customer if the investment yields a good return.

In the conventional approach, power converters are designed according to some performance specifications and usually the economic feasibility of a design proves itself as it finds success in the market based on field experience. In [12] as done in various other resources, the economic feasibility of a converter is evaluated after a design is completed and its commercial success is promoted prior to field experience. In the proposed approach in this work, the design and economics are considered together such that a further step is taken towards cost reduction, as the application field is specified and has impact on the design.

II. System Modeling and Grid Interface

In this paper, design of low-voltage high-power applications is focused, yet the converters employed in wind turbine (WT) applications are used to represent the system modeling where PV applications can be used interchangeably. The bottom part of Fig. 2 demonstrates the focus of this paper whereas upper side depicts the WT with full-scale converter. The part highlighted with dotted dashed line is beyond the scope and is represented with a dc current source, modeling the output current of generator-side ac/dc converter. In Fig. 2, the 2L-VSC is used to elaborate the structure of grid-side dc/ac converter, but all three converter legs of it shall be replaced with the 3L leg modules of Fig. 3, to obtain the full schemes for the 3L-NPC and the 3L-T VSCs. As evident in Fig. 2 and Fig. 3, the converter legs make the difference whereas all the other components are identical/common. Thereby, common parts are grouped consisting of dc-link capacitor, current/voltage sensors, control hardware, common-mode filter (to suppress EMI) and *dv*/*dt* filter (at converter terminals to prevent overvoltage transients). Additionally, the *LCL*-filter is designed once and is identical in each topology; making it a common element as well. Conversely; IGBT, heat-sink, fast diode (for NPC-type), bidirectional switch (for T-type), and gate driver belong to uncommon parts of each topology.

For the rest of the paper, uncommon hardware elements will be implied as power semiconductor main unit (PSMU) and one leg diagrams in Fig. 3 represent each PSMU revealing IGBTs/switches, fast diodes explicitly whereas unique heat sink designs and gate drivers in each topology are not shown.

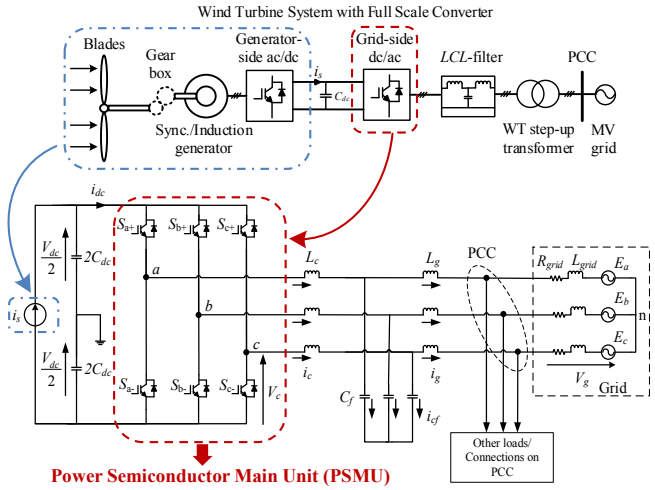


Fig. 2. Grid-connected three-phase 2L-VSC (PCC reflected from medium-voltage (MV) to low-voltage (LV) side).

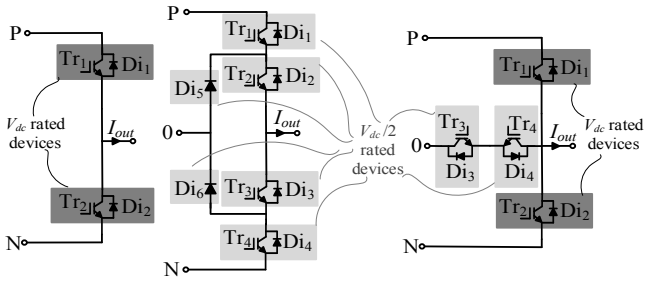


Fig. 3. One converter leg (a) 2L (b) 3L-NPC (c) 3L-T.

III. Proposed Converter Design Optimization Method

Fig. 4 reveals a complete converter design and comparison algorithm where the designation of the switching frequency is also a part of design procedure rather than being a predefined value. The part highlighted as 'three-phase VSC design' is elaborated in [11] where it is built on the verified/tested 2L and 3L-VSCs, displaying detailed information about determination of the switching frequency, *LCL*-filter design (based on selected topology, PWM method and efficiency goal of the design) and grid-compatibility. In this paper, that part is gone through briefly so that the topological comparison part is the primary focus. The algorithm is able to span a wide range of power levels (from tens of kW to multi-MW) under diverse converter topologies and PWM methods, involving the design of grid-side dc/ac converter, and *LCL*-filter (Fig. 2) and ensuring the grid-compatibility via the widely used grid codes. When it comes to the selection criterion for the best topology

(among the examined types) under the chosen PWM pattern (where modulation index (m_i) range determines the optimal/possible PWM patterns [11]), it is based essentially on the ROI of the total investment on the grid-side VSC (i.e. TCO). By definition, TCO is the economic value of a plant over a determined life time, containing initial costs and operating costs. In this paper, for simplicity, maintenance and operating costs are assumed equivalent for each topology, thus they are omitted since the impact on the differential comparison between the TCOs becomes zero. Thus, the TCO term stands for initial cost only, or hardware cost of PSMU, in this paper. Yet, the algorithm is suitable to cover a more comprehensive analysis by expanding the TCO definition. To further simplify the TCO comparison, common components in each topology can be omitted since they would only contribute as offsets to calculations, reducing it to the comparison of only the PSMU components. For each design case, the ROI is calculated and the case providing the shortest ROI is highlighted as the optimal solution. To make a fair comparison and to select the optimal PSMU based only on the ROI; output of all topologies (PSMUs) should yield a unique solution ensuring identical quality on the grid-side current in terms of total harmonic distortion THD_i. However, equivalent output (compatible to the grid codes) for each PSMU is yielded under different efficiencies. Thus, the difference in the efficiencies (i.e. saved losses) can be used to assess the difference in the ROIs regarding the corresponding energy price where the facility is to be established.

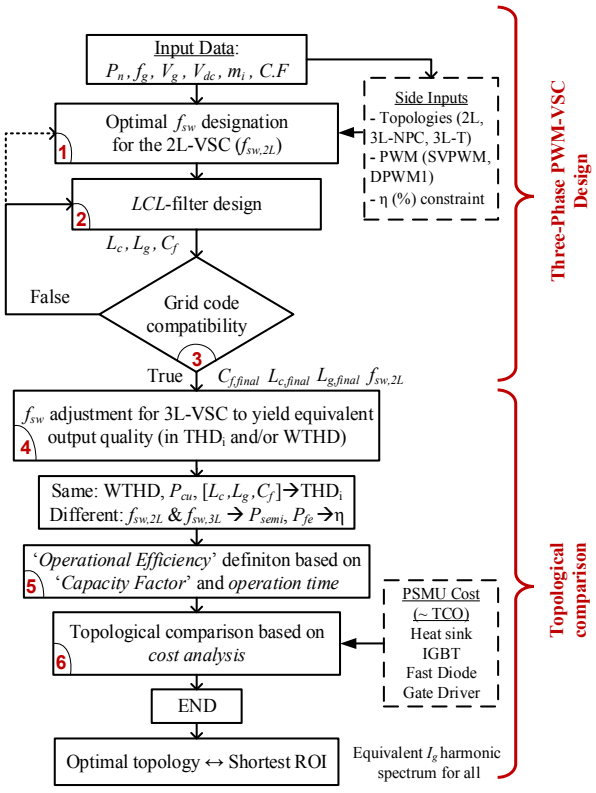


Fig. 4. Complete design flow diagram (dashed boxes provide supplementary information for the related step).

The converter comparison part of the algorithm consists of three key parts as presented by the flow diagram in Fig. 4: switching frequency adjustment for 3L-VSC to achieve equivalent output with that of 2L-VSC, calculation of the operational efficiency, and topological comparison based on the operational efficiency (i.e. saved losses) and the TCO.

As an overview to the entire algorithm, first, suitable semiconductors are selected for the 2L, the 3L-NPC and the 3L-T topologies regarding the input parameters: Power rating (S_n), dc bus voltage (V_{dc}), grid frequency (f_g), grid voltage (V_g), and power factor (PF). Then, the optimal switching/carrier frequency (f_{sw}) is designated with regard to the efficiency constraint under the favored PWM pattern. Second, *LCL*-filter design is provided based on the 2L topology, including filter stability analysis. The grid-side current examination to investigate its compliance with the stringent requirements of the grid codes takes place in the third step. If the requirements cannot be fulfilled, then a new set of filter parameters is selected or a higher f_{sw} is designated. Fourth, f_{sw} for the 3L-NPC and the 3L-T is optimized so that all topologies could yield a unique solution providing equivalent quality on the grid-side current using the same *LCL*-filter designed in the former step. It is important to note that each topology delivers the same quality output with a different efficiency. To compute the mean efficiency of each topology, *operational efficiency* is introduced by using the terms *capacity factor* and *operation time* in the fifth part. In the final part, the TCO of each topology is compared with the accumulated profit over the specified operation time. Then, the topology with the minimum ROI is selected as the optimal solution. Owing to this design algorithm, the ROI becomes the only parameter to decide on the optimal topology providing the same unique solution. The following sections comprehensively examine the design algorithm and clarify all of the design steps with elaborated illustrations of a thorough case study and cost estimation analysis. Besides, in the end, design of two additional applications are provided (only outcomes shown partially) following the proposed method and an alternative topological comparison method is discussed briefly. It should be underlined that the algorithm in Fig. 4 displays three PSMU topologies and two modulation patterns that are of concern. Yet, any topology and modulation method can be assessed by following the same path. Furthermore, starting the process with 2L-VSC is not a requisite. The process can be started with either 3L topology and at the fourth step, f_{sw} for the 2L-VSC could be adjusted likewise.

IV. Converter Design Part

This section considers the design of grid-side dc/ac converter including the *LCL*-filter design (see Fig. 2) via a case-study parameters of which are revealed in Table I. Throughout the procedure, a simulation circuit constructed in Simplorer® is made use of together with Matlab®.

A. Designation of the Optimal Carrier Frequency

First, suitable semiconductors, efficiency constraint and modulation scheme are determined for each topology. Semiconductor and PWM method selections are done considering the input data. First, state of the art commercial industrial converter products are surveyed in detail and generic efficiency values are set to determine the efficiency constraint

in the design according to the power rating of the converter. Once the efficiency range that the converter should be operating at is known, the confined region of the switching frequency is obtained since all the predominant loss mechanisms such as semiconductor loss, *LCL*-filter loss (to be elaborated in Section *V-B*) and damping loss (if any) are taken into account. Therefore, the design sequence involves the determination of efficiency first, switching frequency second, and then the cooling system. For the semiconductor loss calculation, the methodology to calculate switching and conduction losses of semiconductors in a computer simulation environment provided in [13] was adopted. It can be embedded in any design regardless of the simulator as long as the circuit employs ideal switches. For multi-megawatt VSC designs, 0.5 - 5 kHz is the range, roughly, meeting the efficiency constraints of the commercial industrial products regarding all the dominant loss mechanisms [11].

TABLE I
1 MVA LV RENEWABLE ENERGY SYSTEM PARAMETERS

Parameter	Notation	Value
Rated power	S_n	1 MVA
Grid line voltage	V_g	690 V_{rms}
Grid frequency	f_g	50 Hz
DC bus voltage	V_{dc}	1070 V
Efficiency constraint	η	$\geq$ 98.5%

For the revealed system parameters in Table I, 1700V/1200A rated commercial IGBT modules were selected for the 2L (Tr_1-Tr_2) and 3L-T (Tr_1-Tr_4) topologies. Besides, 1200V/1200A switches were picked for the active bidirectional switch part (Tr_2-Tr_3) in the 3L-T. 1200V/1200A IGBT modules (Tr_1-…-Tr_4) and fast diodes (Di_5-Di_6) were opted for the 3L-NPC. For the 1 MVA VSC, all the passive losses (including filter, damping (if any) and other resistive losses) are limited to maximum value of 0.005 pu (0.5%) at full load and this value shifts the efficiency curve down with an offset accounting for a 0.5% decrease at full load. Thus, the optimal switching frequency (i.e. carrier frequency) for the 2L-VSC ($f_{sw,2L}$) arises as $f_{sw,2L} \leq 2.5$ kHz where it yields a rated efficiency of η (%) $\geq$ 98.5%. Likewise, the optimal switching frequency for the 3L-VSC ($f_{sw,3L}$) turns out as $f_{sw,3L} \leq 3.5$ kHz, yielding far less distortion of grid-current (I_g) than the 2L-VSC does. It should be noted that when determining f_{sw}, there should always be a margin to compensate for the additional losses due to overload condition (grid under-voltage case at full-load). Thus, with a reasonable margin, switching frequency for the 2L-VSC is designated as $f_{sw,2L} = 2$ kHz and this value is adopted in the next filter design step. In this paper, the two popular PWM methods containing zero sequence signal injection, namely SVPWM and discontinuous PWM1 (DPWM1), are examined under "*equal switching loss*" principle. For this purpose, f_{sw} is increased by 50% in DPWM1 method so that the switching count and therefore the switching losses could remain the same while ripple of DPWM1 becomes slightly less than that of SVPWM [11]. Picking f_{sw} as 2 kHz for SVPWM and 3 kHz for DPWM1 verifies the theoretical assumption ensuring "*equal switching loss*" ($\eta_{SVPWM} \approx 98.60\%$ and $\eta_{DPWM1} \approx 98.62\%$).

B. LCL-Filter Design and Evaluation of Its Effectiveness

The connection to the electric utility is provided through *LCL* line filters. *LCL* filter is favorable due to its smaller size and weight as well as the improved dynamic response owing to the third order characteristics [1]-[7]. In spite of these prevailing advantages over *L*-filters, the utilization of *LCL*-filters makes the control design challenging. Because, the presence of *LC* part brings a resonant pole pair at the resonant frequency (f_{res} or ω_{res} in Hz and rad/s, respectively) given by

$$\omega_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}}, \tag{1}$$

where L_c, L_g and C_f are converter-side inductance, grid-side inductance, and filter capacitance, respectively.

The conventional design procedure focuses on confinement of resonant frequency within the interval of $10f_g < f_{res} < 0.5f_{sw}$ to achieve the elimination of interface between the switching harmonics and the resonance harmonics [1], [2]. Although this approach is valuable for the systems with high switching frequency, it might become impractical for high power (multi-MW) applications utilizing low switching frequency in the range of a few kHz. In this case, confining the resonant frequency in the interval of $10f_g < f_{res} < 0.5f_{sw}$ might result in bulky filter components, i.e. bulky filter inductors. Thus, the resonant frequency must be set by the designer regarding the severity of the specifications (grid codes) and in some cases f_{res} can be located slightly out of this interval by compromising the attenuation while cost and weight of the filter is somewhat reduced. As evident, the location of the resonant frequency has great impact on stability as well as the attenuation capability of the filter [11]. The most optimal damping technique, which optimizes the filter size and attenuation performance, for the defined resonant frequency region (i.e. low/high resonant region) relies primarily on the preferred current feedback variable [3], [6]. For this reason, the grid-current feedback (GCF) and the converter-current feedback (CCF) methods yield distinct *LCL*-filter parameters depending on the location where the resonance frequency dwells. Priority of the design in terms of cost or performance under the preferred current feedback variable determines the location where the resonance frequency should reside. Therefore, the favored current control method (CCM) is also an input to the *LCL*-design procedure. The calculation of damping ratio ζ depends on the favored current control method along with the preferred damping technique (active damping AD, passive damping PD or inherent damping ID) [11].

Having implemented the proposed filter-design algorithm in [11] yielded the resulting filter components shown in Table II. As a remark, L_g, in this, paper, contains the grid-impedance and transformer leakage inductance. For a short-circuit ratio SCR of 20, grid impedance becomes 5%. Besides, the filter is connected from, low-voltage (LV) to medium-voltage (MV) grid via the step-up transformer (Fig. 2). This transformer has a leakage inductance typically around 5%. Hence, the minimum effective grid-side inductance is assumed 10% (0.1 pu) and it does not contribute to the filter volume [9]. In the filter design stage, GCF control was favored throughout simulations and the capacitor current AD method was able to

stabilize the 2L-VSC system at 2 kHz ($500 < f_{res} = 795 < 1000$ Hz) under the preferred modulation scheme SVPWM.

The power quality injected into the grid should comply with the stringent grid standards whereas the internal design of the grid-side VSC should dictate the maximum peak current ripple (Δi_{max}) to be confined to 10-25% of rated peak load current (I_{load}) (or 20-50% peak-to-peak) [9], [11]. If either of the requirements is not met, one or both of the inductor values and/or the resonant-pole frequency are necessarily increased. Thus, the *LCL*-filter design step is revisited (see Fig. 4).

TABLE II
1 MVA LV RENEWABLE ENERGY SYSTEM LCL-FILTER PARAMETERS

Parameter	Notation	Value
Converter-side inductance	L_c	242 μH (0.16 pu)
Grid-side inductance	L_g	242 μH (0.16 pu)
Filter capacitance	C_f	332 μF (0.05 pu)
Resonant frequency	f_{res}	795 Hz

Reference [11] provides an approach that takes the favored converter topology and modulation pattern into account to estimate the worst-case converter current ripple. Investigation of the grid-side specifications are extended as follows.

Most of the TSOs dictate that the wind-turbines meet the German Electricity Association (VDEW) standard for generators connected to a medium-voltage network [14]. The maximum allowed values for harmonic current components ($I_{v,\mu,allowed}$) allowed by VDEW can be calculated by multiplying the constants ($i_{v,\mu,zul}$) shown in [14] by the short-circuit power SCC (i.e. SCR·S_n) at the connecting point using

$$I_{v,\mu,allowed} = i_{v,\mu,zul} \cdot \mathrm{SCR} \cdot S_n . \qquad (2)$$

The ladder like solid black line in Fig. 5 depicts the current harmonic limits for the simulated system dictated by VDEW, whereas the lower solid red line highlights even stricter limits for non-integer harmonics. Blue vertical lines stand for the magnitudes of obtained harmonic current spectrum acquired from the full system simulations. Even though the filter design ensures a stable controller operation, the severe limits dictated by VDEW might not be met for several harmonics. Besides, a low switching frequency leads to an extremely low control bandwidth, hindering the effectiveness of AD methods. Additionally industrial products cannot merely rely on AD, or ID provided by converter-current control method at low f_{sw}'s [11]. Thus, the usage of a damping resistor, even though its value is lower than that of a system relying only on PD, is more favorable and reliable. For this purpose, 0.11 pu damping resistors are used in series with the filter capacitances. As evident in Fig. 5, the designed filter meets the standards by a sufficient margin. As long as the requirements for the converter current ripple (10-25%) and grid current ripple (VDEW) are fulfilled, the designed *LCL*-filter can be assumed as a qualified and suitable grid interface.

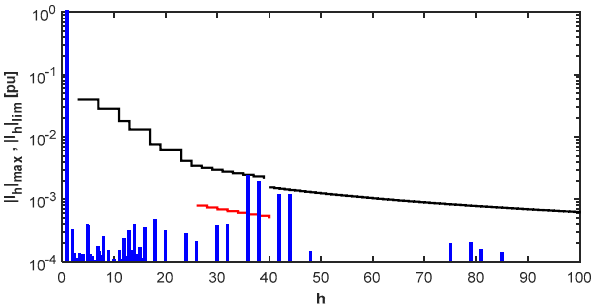


Fig. 5. Worst case pu current harmonic spectrum plotted against the VDEW harmonic-current limits for grid-connected VSCs (SCR = 20).

V. TOPOLOGICAL COMPARISON PART

This section unveils the main contribution of this paper where cost and operating factors (i.e. economic feasibility) are combined with the hardware design phase using the terms of TCO and ROI. As implied in Section III, hardware based topological comparison is simplified/reduced to the comparison of PSMU components (as everything else remains the same). Fig. 6 illustrates the common and uncommon parts of the design procedure for each topology. Consequently, the TCO and the ROI analyses are performed only for PSMU in each design. As presented in Fig. 6, each PSMU structure yields the equivalent current harmonic spectrum at a different efficiency. The cost savings owing to the saved losses/energy (by the difference in efficiencies) become of primary concern in the ROI calculation. Regarding the energy price of the application site, the topology providing the minimum ROI is selected as the optimal solution.

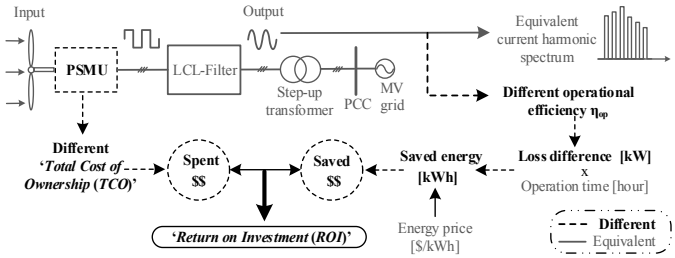


Fig. 6. Topological comparison methodology.

A. Achieving Equivalent Output Performance

As a remark, under the same switching frequency the effective f_{sw} of 3L topologies is nearly twice as high as $f_{sw,2L}$ due to the resulting impact of level increase. Therefore, $\mathrm{THD_i}$ of the 3L topologies is much lower than that of the 2L at the same f_{sw} [11]. However, the target of the converter design algorithm is to provide equivalent output current harmonic spectrum ($\mathrm{THD_i}$ is the aggregate indicator) regardless of the topology using the same *LCL*-filter parameters. To achieve the equivalent current harmonic spectrum on the grid-side, the switching frequency of 3L-VSC, $f_{sw,3L}$ is decreased sufficiently so that the effective switching frequency enhancement brought by level increase is nullified. Hence, the *LCL*-filter is exposed to the same input ripple waveform and exhibits the same attenuation since each PSMU is adjusted to perform equivalently and generates equivalent square waveforms (provided that the system stability is retained). For this purpose, "*weighted total harmonic distortion* (WTHD)" value of converter voltage waveforms of each topology can be computed to verify equivalency. It is different than the classical THD calculation since the output line voltage WTHD calculation contains the effect of orders of harmonics, not the

magnitudes of all harmonics as themselves. Reference [11] can be checked for details regarding WTHD. Besides, THD_i of grid-side current is also a good indicator to monitor the output current quality since it represents an aggregate level of current distortion considering each single harmonic component. It is always a recommended practice to obtain the system behavior against various converter-side inductance L_c (or total inductance L_c+L_g) as revealed in Fig. 7 - Fig. 8. This way, THD_i vs. filter inductance characteristics of each topology is presented as an envelope rather than a single value (i.e. value yielded under the rated inductance) which might otherwise mislead the designer. In the following subsections, this procedure is exemplified under both SVPWM and DPWM1 to show the validity of the model under any modulation pattern; whereas, no performance comparison is made in this article.

1) SVPWM

The red-dashed solid line in Fig. 7(a) shows THD_i performance of 2L-VSC against L_c variation at $f_{sw,2L}$ = 2 kHz. Since THD_i of 3L-VSC is much lower at 2 kHz (due to higher effective frequency), $f_{sw,3L}$ should be varied with reasonable steps to superpose THD_i characteristics. For this purpose, a set of $f_{sw,3L}$ varying within the range of 500 Hz-3 kHz is used and then the optimal $f_{sw,3L}$ is chosen providing the closest THD_i performance to that of 2L-VSC under varying L_c as revealed in Fig. 7(a). The best fitting THD_i curve of 3L-VSC to that of 2L-VSC occurs at $f_{sw,3L}$ = 1 kHz (see Fig. 7(b)), yielding the $f_{sw,3L}$ as half of the $f_{sw,2L}$ as expected.

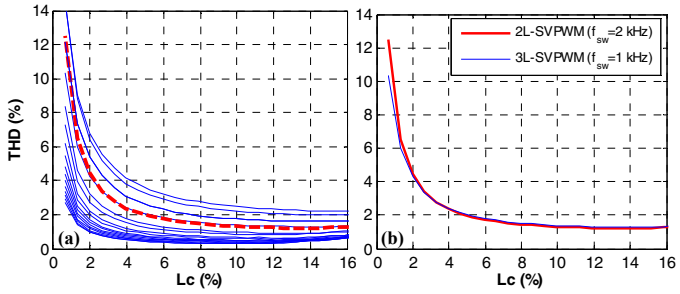


Fig. 7. THD_i(%) vs. L_c under SVPWM (a) $f_{sw,2L}$ = 2 kHz, $f_{sw,3L}$ = 500 Hz - 3 kHz (Increment: 50 Hz) (b) $f_{sw,2L}$ = 2 kHz, $f_{sw,3L}$ = 1 kHz.

2) DPWM1

The same procedure is repeated under DPWM1. The best fitting THD_i curve of 3L-VSC to that of 2L-VSC occurs at $f_{sw,3L}$ = 1.6 kHz as revealed in Fig. 8. Therefore, $f_{sw,3L}$ is found to be approximately half of the $f_{sw,2L}$ as well and the approach to superpose THD_i characteristics is verified to hold under any modulation scheme.

Alternatively, WTHD examination of converter voltage further validates the proposed approach under the specified conditions in Fig. 9 throughout the modulation index (m_i) range of 0.6-1.15 where industrial converters mostly operate [11] (m_i is defined as the peak line-to-neutral V_g over half of V_{dc} with a definition range of 0 - 1.15 for SVPWM and DPWM1). Since m_i = 1.054 in this application, the obtained characteristics in Fig. 7 and Fig. 8 are coinciding with the portion of overlapped curves in Fig. 9.

As mentioned earlier, GCF control was favored throughout simulations and the AD method was able to stabilize the 2L-VSC system under both SVPWM and DPWM1 at f_{sw} =2 kHz. Yet, at the decreased f_{sw} in the 3L, the 3L inverter excites the resonant component along with the PWM sideband harmonics and stability is lost. The GCF control with the AD is not capable of suppressing the resonance as it is not within the current control bandwidth (f_{res} = 795 > 0.5f_{sw} = 500 Hz). Thus, it is mandatory to use PD. As implied previously, industrial products employ PD when f_{sw} is as low as in this case [11]. Hence, 0.11 pu damping resistors are used in series with the filter capacitances to retain the equivalency of the filter for all.

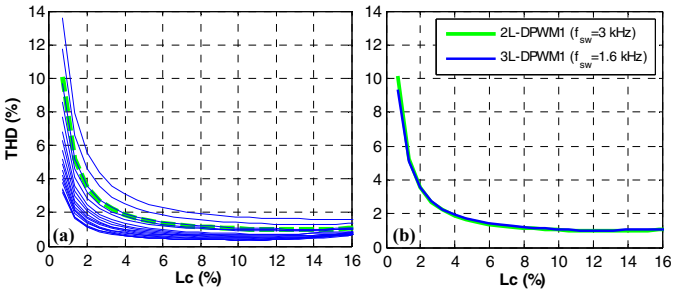


Fig. 8. THD_i(%) vs. L_c under DPWM1 (a) $f_{sw,2L}$ = 3 kHz, $f_{sw,3L}$ = 750 Hz - 4.5 kHz (Increment: 50 Hz) (b) $f_{sw,2L}$ = 3 kHz, $f_{sw,3L}$ = 1.6 kHz.

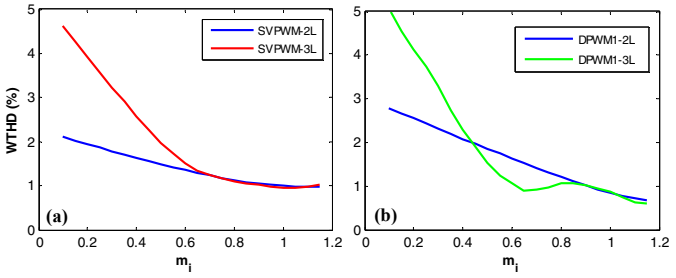


Fig. 9. WTHD (%) vs. m_i characteristics of (a) SVPWM–2L (2 kHz) and SVPWM-3L (1 kHz) (b) DPWM1-2L (3 kHz) and DPWM1-3L (1.6 kHz).

B. LCL-Filter Loss Modeling

LCL-filter loss is another significant loss mechanism in grid-connected converters. All the passive losses (including filter, damping and other resistive losses) in this model are limited to max 0.005 pu (0.5%) at full load to design feasible filters while keeping its size and cost moderate [11]. In the *LCL*-filter, the losses (P_{filter}) are predominantly inductor losses (the losses due to ESR of the filter capacitor may be considered as a part of the PD resistor losses, when present). Thus, in the design, only inductor losses are modeled by

$$P_{filter} = P_{fe} + P_{cu} = k_1 + k_2 \cdot I_{load}^{\,2}, \tag{3}$$

where k_1 stands for core loss P_{fe} (W), P_{cu} (W) is copper loss, and k_2 (Ω) represents the equivalent resistance causing the copper loss. Damping losses are not included in filter loss modeling and are regarded separately. The core losses mainly occur in L_c and the ohmic losses occur both in L_c and L_g. The core loss is calculated by multiplication of core volume (Vol) and core loss density ($K \cdot B^{\alpha} \cdot f^{\beta}$)

$$P_{fe} = K \cdot B^{\alpha} \cdot f^{\beta} \cdot Vol, \tag{4}$$

where B and f stand for magnetic flux density swing and operating frequency ($f = f_{sw}$ in this case), respectively. Since equivalent filters are adopted (identical core material, magnetization, volume and so forth – i.e. equivalent $K \cdot B^{\alpha} \cdot Vol$)

for 2L-VSC and 3L-VSC, P_{fe} becomes a nonlinear function of f_{sw} (i.e. $P_{fe} \sim f_{sw}{}^{\beta}$) as evident in (4). Reduced core loss causes prominent differences between the 2L and the 3L. In order not to penalize the 2L in this comparison, the possible minimum β (i.e. $\beta = 2$ [15]) is selected, yielding $P_{fe} = K \cdot B^{\alpha} \cdot f^2 \cdot Vol$ where $K \cdot B^{\alpha} \cdot Vol$ is equivalent for each topology. Typically, the inductors are designed such that the core losses are about 25-40% of the total inductor losses so that the light and no-load losses are balanced and maintained low (targeting a flat efficiency curve) [11]. For this application, a maximum 0.004 pu (0.4%) total filter loss is presumed. Of the total filter losses, for a presumed core loss of 25% at 2 kHz for the 2L, it is further reduced to one fourth of this value (6.25%) for the 3L at $f_{sw,3L}$ =1 kHz due to the quadratic dependency on f_{sw}. Hence, P_{filter} = 0.004 pu ($P_{fe,2L}$ = 0.001 pu, $P_{cu,2L}$ = 0.003 pu) for the 2L-VSC and 0.00325 pu ($P_{fe,3L} = 2.5 \cdot 10^{-4}$ pu, $P_{cu,3L}$ = 0.003 pu) for the 3L-VSC, while semiconductor losses constitute about 0.01 pu and 0.0075 pu, for the 2L and the 3L, respectively. Damping losses due to 0.11 pu resistors bring about 0.001 pu loss for each topology.

C. Capacity Factor and Operational Efficiency

Power converters operating in WTs do not always perform at rated power/load due to intermittent characteristic of wind. Actually the active time, during which there is considerable power generation, stands for a maximum mean power output about 40% of the rated power in recent WT applications. Thus, based on the mean generated power approach, a grid-side converter employed in a WT can operate up to only 40% of the time annually whereas it is idle for the remaining 60% of the time [16]. Thus, a performance (efficiency) assessment of an individual WT regarding only rated power production is not fair. In the literature, there are several operational efficiency definitions such as "*EURO Efficiency*" and "*CEC Efficiency*", weighing five distinct loading levels with predetermined coefficients [11]. However, these criteria are more suitable to evaluate PV applications or small scale WTs. Yet, a novel operational efficiency definition including large power scale WTs should be developed. Power output vs. wind speed characteristic of the corresponding WT is essential to calculate the operational efficiency of the grid-side VSC. MWT62/1.0 (Mitsubishi WT Generator) is selected as the reference product to illustrate the methodology. Its rated power is 1 MW and the grid-side dc/ac converter is designed by considering connection to the low-voltage grid at 690 V line-to-line. To derive the proposed operational efficiency definition, the definition of capacity factor is provided as follows.

1) Capacity Factor

WT manufacturers assess their products regarding the widely used term *capacity factor* (C.F). Capacity factor is a measure of a WT's actual output, which varies with the wind speed over a period of time. Thus, capacity factor is the actual output over a period of time as proportion of a wind turbine or plant's nominal/maximum capacity

$$C.F\,(\%) = \frac{P_{out}}{P_n} \text{ x } 100\%, \tag{5}$$

where P_{out} is the output power and P_n is the nominal power. P_{out} against wind speed curve provided in the product datasheet of MWT62/1.0 is represented in Fig. 10 by a not-to-scale drawing and then is converted into a rectangle-shaped curve without changing the area underneath to ease the numerical calculations.

The rectangular form assumes that the capacity factor is constant within the corresponding wind speed intervals. The gray-hatched slices referenced and weighed by the coefficients of c_1-c_5 in Fig. 10 depict the portions of each wind strength benefited throughout the operation time (no energy harvesting outside 3.5-25 m/s interval). Depending on the magnitude of coefficients, the mean capacity factor is determined by weighing power outputs correspondingly

$$C.F\,(\%) = \left[\frac{1}{P_n} \sum_{m=1}^{z} P_{out,m}\, c_m \right] \text{x } 100\%, \tag{6}$$

where z stands for the maximum number of intervals, m shows each separate region and c_m represents weighting coefficients for each interval from 1 to z. In this exemplary case, z = 5 and $P_{out,1}$ to $P_{out,5}$ stand for 5% to 100% of P_n. The active period of power generation of a WT per annum is denoted with σ where it values the effective period of power production within 0-100%. For instance, σ = 0.6 stands for an effective/maximum operation time of 60% per year where wind speed is between 3.5 - 25 m/s interval. This modeling can be applied to any P_{out} vs. wind speed characteristics provided by different manufacturers, yielding an easy-forward modeling of intermittent input power.

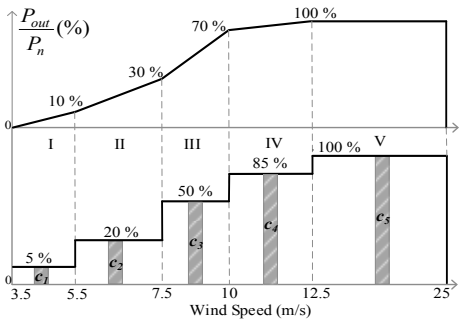


Fig. 10. Power output vs. wind speed (m/s) curve of MWT62/1.0.

2) Operational Efficiency

Since WT is not productive all year long, c_1-c_5 coefficients sums up to σ, i.e. $\sum c_m = \sigma$. However, to build a clearer model for operational efficiency definition, c_1-c_5 coefficients are normalized with σ and a new set of coefficients β_1-β_5 is achieved where $\sum \beta_m = 1$. Thus, the total sum is unity under all circumstances and the correlation in between is represented by

$$\beta_m = \frac{1}{\sigma} c_m \leftrightarrow \sum_{m=1}^{z} \beta_m = \frac{1}{\sigma} \sum_{m=1}^{z} c_m, \tag{7}$$

where the coefficients from β_1 to β_5 represent the normalized weighting coefficients of each wind speed interval during operation time, respectively. For each capacity factor, the coefficients of β_1-β_5 were determined and are tabulated in Table III. As a remark, if (7) is used to convert the disclosed β_1-β_5 coefficients into the c_1-c_5 coefficients by assuming σ = 0.6, then resulting capacity factors on the leftmost column in

Table III can be yielded using (6). Consequently, the proposed operational efficiency η_{op} can be calculated by

$$\eta_{op}(\%) = \left[\sum_{m=1}^{z} \beta_m \eta_m \right] \text{x } 100\%, \quad (8)$$

where η_m is the efficiency of the converter at the specified load (power output) at each specified wind interval/region.

TABLE III
WIND SPEED CLASSIFICATION

C.F (%)	Wind Interval Weighting Coefficients (β_n)				
	β_1 3.5-5.5 m/s	β_2 5.5-7.5 m/s	β_3 7.5-10 m/s	β_4 10-12.5 m/s	β_5 12.5-25 m/s
20 %	0.30	0.40	0.09	0.11	0.10
30 %	0.15	0.25	0.30	0.05	0.25
40 %	0.05	0.30	0.05	0.05	0.55

A wind speed classification as presented in Table III and an efficiency curve against output power percentage are necessary to compute the operational efficiency (η_{op}) of the converter employed in the WT. In order to obtain efficiency curves for each topology, *LCL*-filter loss, semiconductor loss and damping loss (if any) must be taken into account.

3) Derivation of Efficiency Curves against Varying Load

With the implementation of all loss models, Fig. 11 reveals the efficiency curves of 2L, 3L-NPC and 3L-T under varying load/output power, the including overload case. Conduction losses increase faster (quadratic dependency) than switching losses (linear dependency) with increasing load current. As load increases, conduction losses of 3L-NPC rise noticeably since four switches are present along the current path. Therefore, T-type becomes favorable over NPC-type whereas 2L-VSC provides the lowest efficiency under all loads.

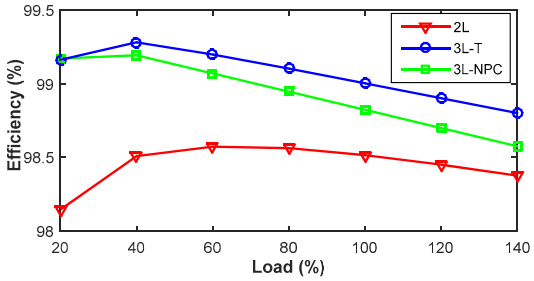


Fig. 11. With the inclusion of loss mechanisms, the efficiency (%) vs. load (%) characteristics for all topologies.

Using the coefficients in Table III and the curves in Fig. 11, calculated operational efficiency of each topology under 20%, 30%, and 40% C.F is tabulated in Table IV. At all capacity factors, 3L-T topology outperformed the other two; whereas, 2L-VSC yielded the lowest efficiency values. In the upcoming section, ROI (i.e. pay-off time) of each topology regarding C.F and the energy price in major energy markets are investigated.

TABLE IV
COMPARISON OF η_{op} (%) AGAINST C.F

C.F (%)	η_{2L}(%)	$\eta_{3L\text{-}NPC}$(%)	$\eta_{3L\text{-}T}$ (%)
20 %	97.49	99.07	99.10
30 %	97.99	99.05	99.13
40 %	98.26	98.98	99.10

D. Cost Analysis

Operation time/schedule of a plant is vital in ROI analysis. As depicted in Fig. 6, to calculate the ROI, the TCO is divided by the overall profit gained during the life time of the plant as given by

$$ROI = \frac{TCO\ [\$]}{Saved\ energy\ [\text{kWh}] \text{ x } Energy\ price\ [\$/\text{kWh}]}, \quad (9)$$

and at the end, the topology providing minimum the ROI is selected as the optimal one.

1) Hardware (PSMU) Cost Analysis

In this section, up-to-date market quotations for the components employed in each PSMU and energy prices (all in US$) are considered to perform cost calculations. IGBTs with 1200 V and 1700 V are priced roughly $530 and $598 per IGBT, respectively. Furthermore, 1200V fast diodes employed in 3L-NPC are determined as $106 per diode, respectively. Gate drive units are accounted for $42 and $86 per channel for 1200V and 1700V respectively. The heat sink design is made regarding the required minimum sink to ambient resistance value ($R_{th(s\text{-}a)}$) found by the detailed temperature analysis that is not shown explicitly in this work. The Aavid heat sinks of 0.028 ˚C/W, 0.06 ˚C/W and 0.3 ˚C/W are quoted at $425, $404 and $270 respectively with an additional cost of $250 for air duct and $400 for blower. The resulting TCO of each PSMU is summarized in Table V. PSMU costs of the 3L topologies are slightly higher compared to the 2L due to the additional components. Besides, initial PSMU cost of the NPC-type is less than that of the T-type. Note that such cost calculations are time and quantity sensitive. Given a time frame and specific voltage and current ratings, through cross-referencing via various manufacturers and distributors, reliable quotes are obtained. Considering the recent stable pricing of components, reliable data is obtained for reliable results to investigate conditions valid over the coming years. Engineers may project different future time frames and include component cost factors based on their experience to obtain results valid for their time frame projection and quantities of product family.

TABLE V
TCO OF PSMU

1 MVA System	2L-VSC	3L-NPC	3L-T
IGBTs	$3588	$6360	$6768
Fast Diodes	$0	$636	$0
Gate Driver	$516	$504	$768
Heat Sink	$2650	$2250	$2250
TOTAL	**$6754**	**$9750**	**$9786**

2) Accumulated Cost Savings Depending on Capacity Factor

In order to assesses the feasibility of the 3L-NPC and the 3L-T as alternatives to the 2L-VSC for low-voltage grid interface applications, saved losses owing to the improved efficiency in the 3L-NPC and the 3L-T over the 2L are determined first. For this purpose, the operational efficiency of each topology under 20%, 30% and 40% C.F is made use of (Table IV) considering 1, 5, and 10 years of operation time to realize short term and long term impacts. Then, the potential cost savings using the saved energy in kWh is calculated. The present value/worth of the future cost savings including a rational annual interest rate in electricity can be calculated by

$$s_0 = \sum_{i=1}^{12n} \frac{s_i}{12\left(1 + k/12\right)^i}, \quad (10)$$

where s_0 is the accumulated cost savings in present value, s_i is cost savings in month i, k is annual interest rate, and n is number of years [10].

VI. Discussion

In this section, two countries in Europe having low and high energy price are evaluated. The net cost paid per kWh by an industrial client in 2014 is 9.41 US ct/kWh (≡ 6.18 pence/kWh) including taxes in Denmark, whereas it is 30.27 US ct/kWh (≡19.89 pence/kWh) in Italy [17]. For instance, the recently designed 2L grid-connected VSC operating at 20% C.F (1752h annually) has 16.1 kW more losses than that of 3L-T, as depicted in Table IV. Thus, 28208 kWh fewer energy losses in 3L-T achieve a cost saving of $s_i \approx$ $2652 per year in Denmark. Then, the accumulated energy cost savings at present value (s_0 's) were calculated regarding the operation times of 1 year, 5 years, and 10 years. The annual interest rate was taken as 5% (k = 0.05). Using (10), $s_0 \approx$ $2581 is worth of $s_i \approx$ $2652 after one year with k = 5%. Table VI is filled with the remaining s_0's correspondingly. Likewise, the same approach was adopted for the comparison between the 2L and the 3L-NPC as well as the cost savings of the systems operating at 30% and 40% C.F both in Denmark and Italy.

Although the 3L topologies cost $3000-3100 more than the 2L, the 3L pay-off the initial PSMU cost difference much shorter than one year. However, C.F and total operation time have a strong impact on the ROI. For instance, if the system operates at 40% C.F for ten years (in average), the 3L-T saves $70001 over the 2L; whereas, the 3L-NPC would save $60184 over the 2L in Italy. Thus, T-type would become the most optimal solution for the implied conditions. Even in the low energy price markets (Denmark) and at low C.F (20%), NPC and T-type pay-off much shorter than one year (more than $2300 is saved per year). It is important to note that, the difference in Fig. 11 becomes higher and higher beyond around 40% load. Yet, much larger differences would be obtained between the 3L-T and the 3L-NPC in Table VI if they were analyzed at heavier loads than 20% - 40% such as full load, but the operational efficiency approach confines the operating points to the left hand side of the efficiency curves where the differences are much less prominent.

TABLE VI
Differential Cost Savings vs. Operation Time in Denmark & Italy

	O.T / C.F	2L vs. NPC			2L vs. T		
		n=1	n=5	n=10	n=1	n=5	n=10
Denmark	20%	$2543	$11535	$20523	$2581	$11709	$20833
	30%	$2541	$11530	$20513	$2727	$12368	$22004
	40%	$2319	$10516	$18710	$2697	$12231	$21761
Italy	20%	$8180	$37104	$66018	$8303	$37665	$67013
	30%	$8175	$37089	$65988	$8770	$39783	$70782
	40%	$7457	$33827	$60184	$8673	$39344	$70001

Developments in the bidirectional switch of the 3L-T are likely to consolidate its superior performance in near future. For instance, a brand-new active bidirectional switch in T-type designed by *Fuji* (4MBI500VG-1800R-50R) eliminates the anti-parallel diodes and diminishes total semiconductor losses by nearly 0.03% in operational efficiency over the conventional T-type under all C.Fs [11].

Two additional applications are also considered adopting the same approach as follows. Only the results are shown in tables where input parameters and the selected semiconductors are tabulated in Tables VII and VIII, respectively. Additional important parameters for the 500 kVA VSC are m_i = 1.045 (SVPWM), $f_{sw,2L}$ = 5 kHz, $f_{sw,3L}$ = 2.5 kHz. Besides, the TCOs of each PSMU are $4338, $4470 and $5257 for the 2L, 3L-NPC and 3L-T, respectively. Similarly for the 2 MVA VSC, m_i = 1.053 (SVPWM), $f_{sw,2L}$ = 1.5 kHz, $f_{sw,3L}$ = 0.75 kHz while the TCOs of each PSMU in this case are $7845, $14199 and $12838 for the 2L, 3L-NPC and 3L-T, respectively.

TABLE VII
LV Renewable Energy System Parameters

Parameter	Application I	Application II	Application III
S_n	500 kVA	1 MVA	2 MVA
V_g	480 V_{rms}	690 V_{rms}	690 V_{rms}
f_g	50 Hz	50 Hz	50 Hz
V_{dc}	750 V	1070 V	1070 V
η	≥ 98%	≥ 98.5%	≥ 99%
$L_c = L_g$	62 µH (0.042 pu)	242 µH (0.16 pu)	215 µH (0.28 pu)
C_f	207 µF (0.03 pu)	332 µF (0.05 pu)	669 µF (0.05 pu)
R_d	0 Ω	0.06 Ω (0.11 pu)	0.02Ω (0.08 pu)
f_{res}	1.98 kHz	795 Hz	593 Hz

TABLE VIII
Power Semiconductors Utilized in the PSMUs

App. / *SW #	2L & 3L-T	3L-NPC & 3L-T	
	1-2	1-4 (NPC) &3-4 (T)	5-6 (NPC)
500 kVA	600A/1200V [1]1MBI600V-120-50	600A/600V [1]2MBI600-VD-060-50	600A/600V [2]PM600DV1A060
1 MVA	1200A/1700V [3]CM1200HCB-34N	1200A/1200V [3]CM1200HA-24J	1200A/1200V [3]RM1200DB-24S
2 MVA	2400A/1700V [3]CM2400HC-34N	2500A/1200V [3]CM2500DY-24S	2400A/1200V [3]RM1200DB-24S x 2

[1]Fuji, [2] Mitsubishi, [3] Powerex, * With reference to Fig. 3.

Fig. 12(a) and (b) show the resulting efficiency curves obtained for 500 kVA and 2 MVA applications, respectively. Performance results are tabulated in Table IX. Although the numeric n_{op} values are slightly different in all three applications in Tables IV and IX, the amount of saved energy differs remarkably. For instance, even a 0.1% difference yields 500 W, 1000 W and 2000 W saved energy in 500 kVA, 1 MVA and 2 MVA, respectively. Thus, as the power level increases, even a tiny difference results in huge profits in the long run. Table X presents all of the calculated s_0 values in Denmark correspondingly.

In the 500 kVA application, the 3L-T costs about $900 more than the 2L, so in the low energy price markets such as Denmark, the ROI is about 1-2 years. Even in the long run, the gained profit does not reach to high numbers compared to the 1 MVA application. Since the TCO of the 3L-NPC is comparable with that of the 2L, the ROI is much shorter than 1 year. Therefore, in the first two years, the 3L-NPC is a more

attractive solution than the 3L-T. Then, the 3L-T overtakes the 3L-NPC after about two years. However, the situation is totally different for the 3L-T in case it operates in a high energy price market such as Italy. The ROI is less than 1 year at C.F = 20% ($2089) and the gained profit rises with C.F increase such that $2399 is saved over the 2L at C.F = 40% in 1 year. The 3L-T can save $19363 over the 2L in 10 years at C.F = 40% whereas it saves $10150 over the 3L-NPC.

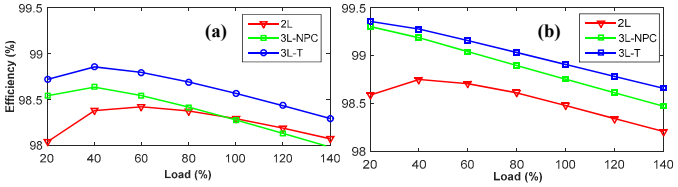


Fig. 12. The efficiency (%) vs. load (%) variation of (a) 500 kVA VSC (b) 2 MVA VSC.

TABLE IX
η_{op} (%) AGAINST C.F (500 KVA & 2 MVA)

C.F \ η_{op}	500 kVA			2 MVA		
	η_{2L} (%)	$\eta_{3L\text{-}NPC}$ (%)	$\eta_{3L\text{-}T}$ (%)	η_{2L} (%)	$\eta_{3L\text{-}NPC}$ (%)	$\eta_{3L\text{-}T}$ (%)
20%	97.39	98.02	98.20	98.08	99.12	99.17
30%	97.86	98.24	98.46	98.35	99.05	99.14
40%	98.09	98.31	98.56	98.45	98.96	99.07

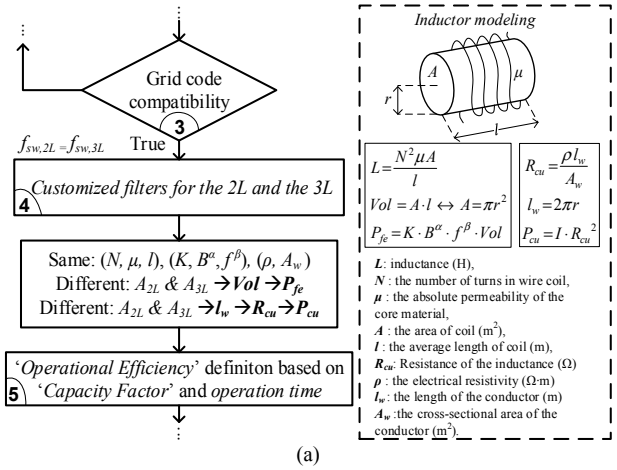
TABLE X
DIFFERENTIAL COST SAVINGS IN DENMARK (500 KVA & 2 MVA)

	O.T \ C.F	2L vs. NPC			2L vs. T		
		n=1	n=5	n=10	n=1	n=5	n=10
500 kVA	20%	$504	$2274	$4063	$650	$2946	$5241
	30%	$460	$2086	$3712	$721	$3270	$5817
	40%	$355	$1610	$2864	$746	$3384	$6020
2 MVA	20%	$3323	$15070	$26812	$3480	$15787	$28088
	30%	$3381	$15335	$27283	$3786	$17172	$30551
	40%	$3905	$17712	$31512	$4615	$20935	$37248

In 2 MVA application, the PSMU cost of the 3L-NPC is the highest since the 1200 V and 1700 V IGBTs were quoted almost identical at such high current ratings. This big TCO difference is reimbursed within 1-2 years in the low energy price markets whereas the ROI is about several months in the high energy price markets (about $11000 savings in 1 year). Apparently, the 3L-T becomes much superior as the power level goes beyond 1 MVA and as the WT operates at higher C.Fs (saves $18000 over 3L-NPC in 10 years at C.F = 40%).

It can be inferred that the 2L-VSC can be more competitive below 1 MVA, whereas the 3L-T holds it superiority in all cases and becomes much superior above 1 MVA. Although it is difficult to set a solid boundary on the power ratings of topologies, the results unveil the trend/power region where the differences become subtler or more prominent. It is also evident that n_{op} difference becomes less effective below 1 MVA and vice versa above 1 MVA, confirming that 2L-VSC is less competitive in high power LV applications. Results also show that the approach of n_{op} is valuable since it defies the expectation that the higher the C.F, the shorter the ROI. Since the saved losses either between the 2L and the NPC or between the 2L and the T might be higher at light loads (see Fig. 11, Fig. 12, and Fig. 14) and the weighting coefficients in Table III are given higher weight at lighter loads to achieve lower C.F. Hence, it is possible to have a shorter ROI in a lower C.F as evident in Tables VI and X. Having higher gaps at lighter loads is mostly due to the larger core loss in the 2L and faster increase of conduction losses (quadratic) than switching losses (linear) with increasing load current (more number of elements present along the current path in the NPC and T increase losses faster as load increases).

The complete design algorithm is also compatible to deliver the optimal topology using different approaches. For instance, the equivalent output (I_g meeting VDEW standards) can also be achieved by fixing the f_{sw} and customizing the filter for the 2L and the 3L individually. In this case, filter volume, weight, cost, and its corresponding losses differ in each topology. For a fair comparison, a filter design method is developed where we assume that filters are made of the same core material, windings, etc. i.e. equivalent $K{\cdot}B^{\alpha}{\cdot}f^{\beta}$. In brief, the filter is designed independently following the steps 1-3 in Fig. 4 for each of the 2L and the 3L where the f_{sw} is not changed. Then, in step 4, the resulting filter components for each topology are yielded as shown in Fig. 13(a). The customized filter elements for the 3L are L_c=L_g= 135μH (0.08 pu) and C_f= 398μH (0.06 pu) at f_{sw}= 2 kHz, yielding f_{res}= 968 Hz < 0.5f_{sw} that achieve stability without the need of PD. (See Table II for the 2L.) Hence, R_d = 0 for both the 2L and the 3L. Following the approach in Fig. 13(a), the calculated values (ensuring equally acceptable output current spectrum–see Fig. 14(a)) are L_{2L} = 242 μH and L_{3L} = 135 μH for the 2L-VSC and the 3L-VSC, respectively where the details are presented in Fig. 13(b). As a remark, total filter loss is 0.00325 pu in the 3L for the equivalent filter approach (in section V. B), thus filter losses in the 3L-VSC have been further reduced (0.0028 pu) in this approach. The gap between the 2L and the 3L-VSCs at lighter loads in Fig. 14(b) increases even further due to the quadratic dependency of copper losses on the load current.



(a)

$$\frac{L_{2L}}{L_{3L}}\equiv\frac{A_{2L}}{A_{3L}}\equiv\frac{Vol_{2L}}{Vol_{3L}}\equiv\frac{P_{fe,2L}}{P_{fe,3L}}\cong 1.8 \rightarrow 14\%\ \text{less}\ P_{fe}\ \text{in the}\ 3L$$

$$\sqrt{\frac{A_{2L}}{A_{3L}}}\equiv\frac{r_{2L}}{r_{3L}}\equiv\frac{l_{w,2L}}{l_{w,3L}}\equiv\frac{R_{cu,2L}}{R_{cu,3L}}\cong 1.34 \rightarrow 56\%\ \text{less}\ P_{cu}\ \text{in the}\ 3L$$

$$\therefore P_{filter,2L}=0.0040\ pu \leftrightarrow P_{filter,3L}=0.0028\ pu$$

(b)

Fig. 13. (a) Modified design flow diagram (only step-4 is different). (b) Resulting core and copper loss differences between the 2L and the 3L.

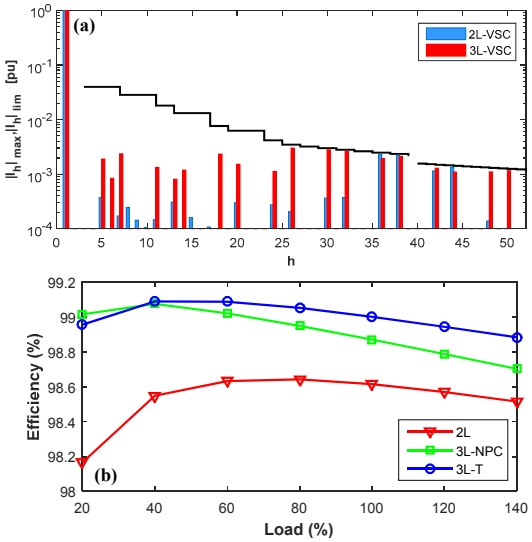


Fig. 14. (a) Worst case pu current harmonic spectrum (b) The efficiency (%) vs. load (%) variation for all topologies (1 MVA with equal f_{sw} approach).

Resulting operational efficiency of each topology under 20%, 30%, and 40% C.F are tabulated in Table XI. Besides, this approach stipulates the inclusion of filter cost to PSMU cost. Regarding both the quotations and the approach in [10], price for a three-phase coil becomes roughly \$14.3/J and the price for three capacitors at this voltage level is roughly \$5/μF. Deducting the aforesaid 0.1 pu aggregate grid-side inductance (transformer leakage + grid inductance) from L_g and adding the corresponding cost of the filter components to the TCO of the PSMU yield the resulting TCO as shown in Table XII.

The TCO of the 3L becomes slightly more expensive than the 2L with the customization of the filter. Hence, slightly reduced gained profits in Table XIII (compared to those in Table VI) is balanced with the reduced TCO difference between the 2L and the 3L-VSCs, where it is still clear that with both approaches the superiority of the 3L topologies has been revealed where T-type has always been the most prominent one. Besides, the weight of the filters employed in the 3L are substantially lighter than those of in the 2L where a rough assumption of 1kg/10μH yields 60 kg difference [10]. The need of a bigger and more expensive cooling for the inductances is another disadvantage of the 2L in this equivalent f_{sw} approach. However, such aspects cannot be fit in the ROI calculation, thus the merit of analytical comparability of the equivalent filter approach must be underlined.

TABLE XI
COMPARISON OF η_{op} AGAINST C.F (1 MVA - EQUAL f_{sw})

C.F (%)	η_{2L}(%)	$\eta_{3L\text{-}NPC}$(%)	$\eta_{3L\text{-}T}$ (%)
20 %	97.52	98.76	98.79
30 %	98.04	98.88	98.90
40 %	98.33	98.90	98.95

TABLE XII
TCO OF PSMU AND THE *LCL*-FILTER (1 MVA - EQUAL f_{sw})

1 MVA System	2L-VSC	3L-NPC	3L-T
PSMU	\$6754	\$9750	\$9786
Inductor	\$3340	\$1350	\$1350
Capacitor	\$1660	\$1990	\$1990
TOTAL	**\$11754**	**\$13090**	**\$13126**

TABLE XIII
DIFFERENTIAL COST SAVINGS IN DENMARK (1 MVA - EQUAL f_{sw})

C.F \ O.T	2L vs. NPC			2L vs. T		
	n=1	n=5	n=10	n=1	n=5	n=10
20%	\$1991	\$9032	\$16070	\$2042	\$9261	\$16477
30%	\$2025	\$9183	\$16339	\$2069	\$9384	\$16696
40%	\$1833	\$8314	\$14793	\$2012	\$9124	\$16233

VII. CONCLUSION

This paper conveys the design of grid-connected renewable power converters taking the economic feasibility of the system into account during the design phase via the terms of TCO and ROI. Considering the capacity factor of a wind energy system or irradiation characteristics of PV systems along with the energy efficiency characteristics of 2L and 3L (NPC and T type) converters in the energy yield during the design stage, the ROI of additional cost of 3L topologies over the 2L can be calculated and the benefit can be clearly illustrated. The design methodology involves the complete design of the system including the converter topology, PWM method, *LCL* filter, control method, etc. The design method involving equivalent *LCL*-filter for the same grid current quality, shows the converter differential cost and energy savings, while the design for fixed switching frequency emphasizes the filter size and cost related differences, both favoring the 3L topologies.

The proposed methodology was tested via 0.5, 1, and 2 MVA renewable energy systems. It was revealed that the 3L is economically feasible in low-voltage multi-MW applications especially in high energy price markets since the ROI of the 3L is much less than that of the 2L. Consequently, the trends for the renewable energy systems favor the 3L topologies (T-type more than NPC type), with the shortest ROI (additional investment for the 3L-T type system compensated in typically much less than 1 year) for most systems where the difference becomes much more prominent beyond 1 MVA ratings.

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