Modeling CMOS PIN Photodiode using COMSOL

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Abstract— **Modeling semiconductor devices has become mandatory in most challenging research activity. Finding a powerful tool that models these devices represents a goal of these users. In this work, Silicon PIN photodiode is designed using complementary metal-oxide semiconductor (CMOS) Technology. COMSOL Multiphysics is the selected challenging tool for simulation and characterization of this design. The adjustment of the proposed model as well as the different outputs like Electric field and Electric potential distribution, I-V characteristics and other parameters are presented. The output current has shown an allure of a current that consists of three regions: Trap-Assisted Tunneling, Band-to-Band Tunneling and avalanche. These current regions in addition to the high value (10^5 V/cm) of the obtained electric field are typical for Silicon Avalanche Photodiodes (SiAPD). The possibility to use this tool for SiAPD analysis and simulation is therefore discussed.**

Keywords: COMSOL, Semiconductors, PIN photodiode.

I. INTRODUCTION

Several tools are used to simulate and/or design semiconductor devices. TCAD is the most traditional tool that is currently used and it was adopted in different publications like in [1]. However, the process to make a full design by this tool is complicated and makes it difficult to use. In addition, this tool only takes into considerations the electric characteristics of the design and not all the physical aspects that exist in the model. This might produce results that did not exactly match with the experimental ones as stated in [2]. Another tool like Coventorware provides also some semiconductor simulations. Unfortunately, these simulations cannot be used to make a suitable design. Although, it permits to make a deposition process but there is no doping process (which is very essential in semiconductor design) can be provided by this tool. Hence, the simulations that are done by this software are likely to be static and never can be kinetic. Synopsis, Silvaco and Ansys are other available tools used in semiconductor simulations but they also suffer from non-adaptability with semiconductor process and functioning like previous cited tools.

COMSOL Multiphysics is a tool that, following to its title, takes into consideration all the physical aspects that exists in the design. The semiconductor model [3], [4] and [5] represent the only available model that treats the semiconductor devices using COMSOL. From this model we have designed a CMOS PIN photodiode after paying high attention in defining the geometry, physics and boundary conditions. The interest of using CMOS technology is its low cost and high integration capacity with the circuit. In addition, modeling a PIN photodiode represents a good background before going further in more complex design like modeling a Silicon Avalanche photodiode (SiAPD) with Premature Edge Breakdown Prevention (PEBP) techniques as in [2].

Silicon PIN photodiodes are used in different kinds of applications. In general, the bulk region of these photodiodes consists of intrinsic silicon. However, in practice this region is slightly doped n-type n^- silicon (usually called PνN), or slightly doped p-type p^- silicon (usually called PπN). A complete design of PνN in 2D and in 3D is presented in section II (the model also functions for a PπN photodiode). The model adjustment and the obtained results are explained in section III.

II. MODEL DESIGN

As all models designed by COMSOL, we have provided the PIN photodiode model the required physical modules, boundary conditions and the proposed geometry. The model is then meshed in order to obtain the required results. Maxwell's equations, Boltzmann transport theory and Neumann boundary conditions are employed to resolve the different equations that exist in semiconductor and to provide boundary conditions between the different junctions. The basic equations that exist in model are expressed in equation (1):

$$\begin{aligned} -\nabla.(\varepsilon\nabla\psi) &= q(p-n+N) \\ -\nabla.J_n &= -qR_{SRH} \\ -\nabla.J_p &= qR_{SRH} \end{aligned} \tag{1}$$

where ψ equals to electrostatic potential, q indicates the elementary charge, n *and* p are the electron and hole concentrations respectively, N represents the fixed charge associated with ionized donors.

The electron and hole current densities, **J**n and **J**p (2), are expressed in terms of ψ, n and p:

$$\begin{aligned} J_n &= -qn\mu_n\nabla\psi + qD_n\nabla_n \\ J_p &= -qn\mu_p\nabla\psi - qD_p\nabla_p \end{aligned} \tag{2}$$

where μ_n and μ_p are the carrier mobilities, D_n and D_p are the carrier diffusivities.

Shockley-Read-Hall recombination is represented by the term R_{SRH} (3), which is a general recombination process using traps in the forbidden band gap of the semiconductor.

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$$R_{SRH} = \frac{np - n_i^2}{\tau_p(n+n_1)+\tau_n(p+p_1)} \quad (3)$$

where n_i is the intrinsic carrier concentration, τ_n and τ_p are the carrier lifetimes, n_1 and p_1 are equal to n_i.

The boundary conditions are expressed in equation (4)

$$\psi = V_a + \frac{\kappa T}{q}\ln\left(\frac{\frac{N}{2}+\sqrt{\left(\frac{N}{2}\right)^2+n_i^2}}{n_i}\right), \quad n = \frac{N}{2}+\sqrt{\left(\frac{N}{2}\right)^2+n_i^2} \quad (4)$$

$$p = -\frac{N}{2}+\sqrt{\left(\frac{N}{2}\right)^2+n_i^2}, \qquad n_i^2 = np$$

where Va is the applied voltage which is going to be varied with a small step ΔV.

At each value of Va, the current densities J_n and J_p are calculated using Lagrange multipliers that already exists in COMSOL. A more detailed description about the physical equations and the boundary conditions in addition to complete Silicon properties are explained and shown in [3].

The two electrodes in [3] are placed opposite to each others. We have designed the two electrodes N^+ and P^+ to be at the top of the substrate to be adapted with CMOS technology. The p-type doping profile is considered to have a negative sign while the n-type doping profile is considered to have a positive sign. The doping concentration N is approximated with an exponential functions as in (5) in addition to the slightly doped type.

$$f(a,b,k) = e^{\left(-\left(\frac{a}{ch}\right)^2\right)} * \left(\left(|b|<\frac{k}{2}\right)+\left(|b|\geq\frac{k}{2}\right)*e^{\left(-\left(\frac{\left(|b|-\frac{k}{2}\right)}{ch}\right)^2\right)}\right) \quad (5)$$

Hence N can be expressed as:

$$N = N_v + NDn\max * f(y, x-d_{cathode}, e_{cathode}) + NDn\max * f(y, x+d_{cathode}, e_{cathode}) - NAp\max * f(y, x, e_{anode}) \quad (6)$$

where N_v represents the slightly doped n^- silicon (replaced by $-N_\pi$ in case of slightly doped p^- silicon), NDnmax and NApmax represents N^+ (maximum n-type) and P^+ (maximum p-type) respectively, $e_{cathode}$ and e_{anode} represents the cathode and anode dimension respectively, $d_{cathode}$ corresponds to the distance from the midpoint of e_{anode} to the midpoint of $e_{cathode}$, ch is the doping fall-off constant and it is expressed by (7) as:

$$ch = \frac{ju}{\sqrt{\log\left(NAp\max / N_v\right)}} \quad (7)$$

where ju represents the junction depth.

The geometry of the 2D model is built in the xy plane. The PIN photodiode approximates 30 µm along x-axis and 3.4µm along y-axis. The anode approximates 10 µm at the middle of the substrate along x-axis and the cathode approximates 3 µm and designed to be some distance far from the anode extremity. The applied voltage Va is placed on the anode, and the cathode is supposed to be grounded. High attention is paid while variation of Va as the model might not converge. A small initial value (typically zero) and a small step ΔV (typically of order 10^{-2}) might avoid the non convergence of the model.

Once the geometry is defined, we mesh the design as shown in Fig. 1. We have done higher refinement to the meshes that are located near the cathodes and near the anode with respect to other meshes that exist in the system as they contain most of the physical and boundary conditions.

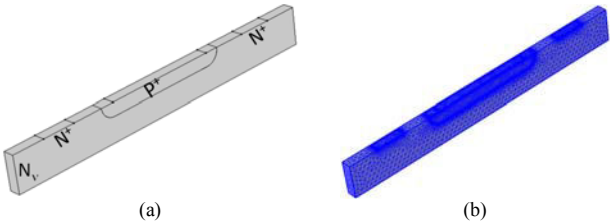
Most designers are satisfied in 2D simulations as they take the third dimension following to the technology limit (0.35 µm or 0.18 µm, etc..). COMSOL provides the possibility to make a 3D simulation. In our model, once the 2D design in the xy plane is done, we extrude the design along the z-axis. Then we add the physical and boundary conditions to the new design. Fig. 2 shows the overview of the model in 3D of PvN before and after meshing.

For the 3D design, we have reproduced exactly the same physical equations and boundary conditions in 2D as we haven't assumed any variations along the z-axis.

III. Results and Discussions

The model consists of different input parameters (geometry, doping concentration, applied voltage, etc..) that influence the obtained results. In addition, the model can provide different output parameters (Electric field, Electric potential distribution, etc..). For simplicity, we will study the variations of PIN structure on the output electric field. Fig. 3 depicts the PIN and the associated variables to be varied.

Figure 1: Model mesh of PIN.



(a) (b)

Figure 2: Overview of the PIN model in 3D (a) before meshing (b) after meshing.

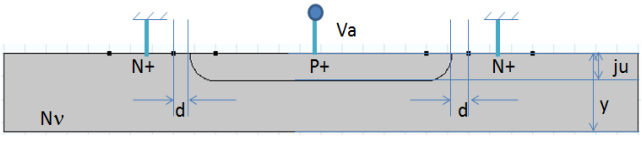


Figure 3: The PIN model where ju is the junction depth, d is the gap between two electrodes, y the thickness of the substrate under study, Va is the applied voltage, N^+ and P^+ are maximum n-type and p-type doping concentration, N_v represents the slightly doped n^- silicon

A. *Model Adjustments*

The model adjustment was studied without taking into account the state-of-the-art of any fabrication technology in order to have a complete overview whatever the technology adopted is. We have supposed $N_v = 10^{15}$ cm^{-3} and $N^+ = P^+ = 10^{17}$ cm^{-3} and we have applied a variable reversed bias voltage along Va. We have studied the influence of the gap between two electrodes (d), the junction depth (ju), and the PIN thickness along y as shown in Fig. 3 on the electric field.

- Influence of the gap between two electrodes (d)

The distance between the electrodes is governed by the technology that will be applied (0.35µm, 0.18µm, etc..). However, when technology permits, it is important to know what the best position of the electrodes is. The electric field was calculated for different distance (d) between P^+ and N^+ and the results are shown in Fig. 4. The electric field increases as the distance (d) decreases. In addition, Fig. 4-a shows an electric field near to an avalanche electric field.

- Influence of the junction depth (ju)

Following to Silicon absorption length, the light with longer wavelength can penetrate to the deeper junction which allows the incident light with longer wavelength to excite electron-hole pairs at the deep regions. In some applications of image sensor, it is important to have a photo receiver that detects all visual light. Following to [6], the blue, green and red light photodiodes must have a junction depth of 0.1 nm, 1.1 nm and 2.1 nm respectively. The electric field for these three different junction depths is shown in Fig. 5.

- Influence of different thickness (y)

Like precedent statement, it is also important to know what the best thickness of substrate is when technology permits. The electric field was calculated for different thickness (y) and the results are shown in Fig. 6. The electric field increases as the thickness (y) increases.

We have studied the influence of variation of the PIN structure on the electric field. The same variations were noticed while using a PπN photodiode. The high values of the electric field were seen at the junction peripheral edges and this will produce premature breakdown of the device [7]. The resolution of this problem represents our future work.

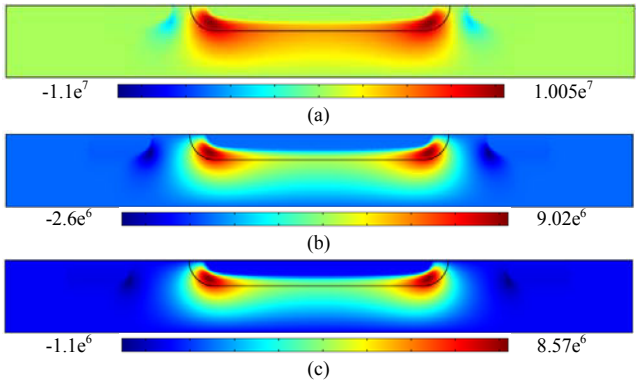


Figure 4: The electric field for (a) d=1 nm (b) d=2 nm (c) d=3 nm and the corresponding electric field bar in V/m.

Other tools are more powerful than COMSOL in semiconductor simulations as shown in Table 1. Hence, it is preferable to use this tool in combination with others tools in order to have a complete device design.

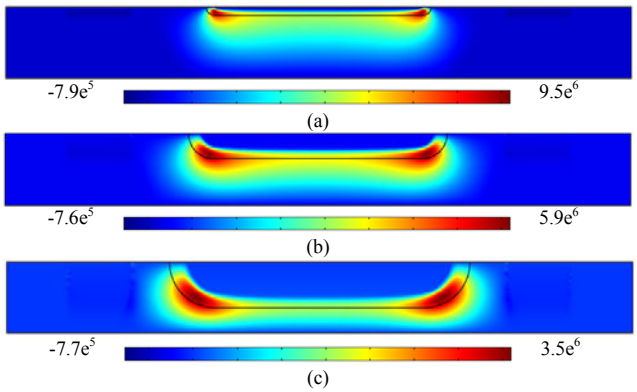


Figure 5: The electric field for (a) ju=0.1 nm (b) ju=1.1 nm (c) ju=2.1 nm and the corresponding electric field bar in V/m.

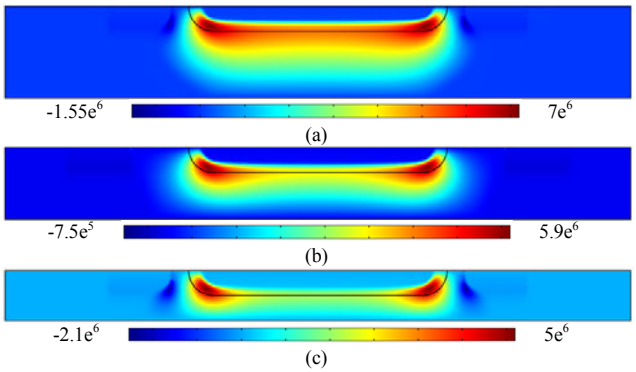


Figure 6: The electric field for (a) y=4.2 nm (b) y=3.2 nm (c) y=2.2 nm and the corresponding electric field bar in V/m.

TABLE I. COMPARISON BETWEEN DIFFERENT TOOLS IN SEMICONDUTOR SIMULATIONS

Tool / Parameter	COMSOL	TCAD	MATLAB	ANSYS
Facility to produce the model	Excellent	GOOD	POOR	GOOD
Calculate all parameters together	GOOD	POOR	Excellent	GOOD
Speed	Excellent	GOOD	POOR	GOOD
Complexity Level	Low	Very High	Low	Moderate
Cost	High	Moderate	Low	Moderate
Reliability	GOOD	Moderate	Moderate	Moderate
Matching with CMOS Technology	POOR	Excellent	POOR	POOR
Optics adaptability	Excellent	POOR	GOOD	Moderate
Optoelectronics adaptability	Moderate	Moderate	GOOD	POOR
Hardware Link	GOOD	POOR	GOOD	GOOD

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B. *Simulated Outputs*

In this section we present some of the output results that can be obtained by the model. We have studied the PIN photodiode of Fig. 5-b (Green PIN).

- Doping concentrations

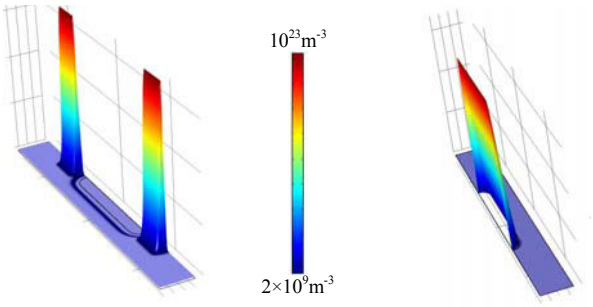
We have introduced a doping profile as in equation (6). The model has reproduced the doping profile n and the doping profile p of equation (1) exactly as they are introduced as shown in Fig. 3. The two maximum n-type (N^+) are at both extremities and are shown in Fig.7-a. The maximum p-type (P^+) at the middle of the substrate is shown in Fig. 7-b

- Electric Potential

We have calculated the electric potential distribution of the PIN in 3D. The distribution almost disappears around 0.7V (silicon threshold voltage) as shown Fig. 8-b, while it is very high in forward bias around P^+ as shown in Fig. 8-a and also very high in reversed bias around N^+ as shown in Fig. 8-c .

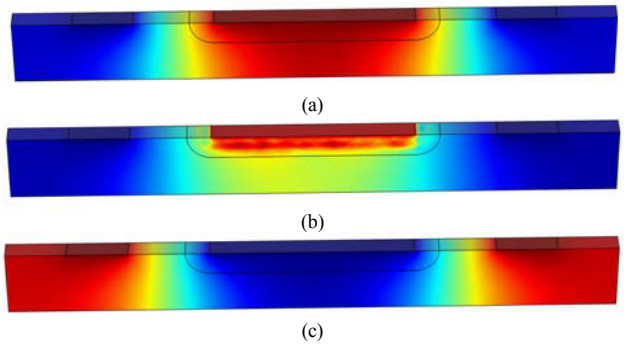
- The I-V characteristics

The reverse bias voltage is only considered while studying the I-V characteristic of the photodiode. Fig. 9 shows a breakdown voltage of about 22V. This potential is relatively high to be used in CMOS technology. However, it shows an allure of a current that consists of the following zones: (from 0V to -15V) Trap-Assisted Tunneling, (from -15V to -22V) Band-to-Band Tunneling, and (after -22V) the avalanche zone.



(a) (b)

Figure 7: The doping concentration of (a) n-type (b) p-type of the PIN.



(a)

(b)

(c)

Figure 8: The variation of the electric potential distribution (a) in forward bias (b) around the threshold voltage (c) in reversed bias.

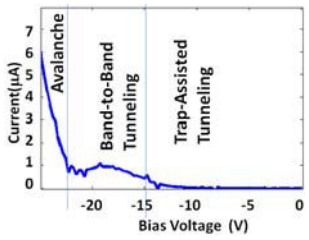


Figure 9: The I-V characteristics of the PIN in reversed bias.

These zones are very interesting as our future work is to design a SiAPD photodiode. In addition, the value of the electric field is in order of 10^5V/cm as shown in Fig. 4-a. This high value represents the beginning of the avalanche zone of Silicon photodiodes. The introduction of n/p-well or deep n/p-well will reduce the premature breakdown and also the breakdown voltage till around 10V as in [2].

IV. Conclusion

We have modeled and characterized a PvN photodiode in CMOS technology using COMSOL. As long as the physical and boundary conditions are well defined, this tool can provide an easy way to simulate a very complex subject like semiconductors design. In addition, it allows creating or modifying the model in relatively quick time compared to other tools. Modeling a Silicon avalanche photodiode for Near InfraRed Spectroscopy (NIRS) will be the perspective work. Therefore, a good declaration of the Premature Edge Breakdown Prevention (PEBP) techniques must be employed in order to obtain a low breakdown voltage and a very high electric field situated just under the active area and not only at the junction peripheral edges.

Acknowledgment

We gratefully acknowledge the financial support from the Canadian Institutes of Health Research (CIHR) and CMC Microsystems.

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