IECON2015-Yokohama
November 9-12, 2015

Single-DC-Source 7-Level CHB Inverter with Multicarrier Level-Shifted PWM

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***Abstract*—This paper presents a 7-level cascaded H-bridge (CHB) multilevel inverter using a single DC source. The second DC bus is a capacitor that its voltage is controlled by switching sequences. The capacitor voltage is regulated at half of the DC source amplitude to have seven voltage levels at the output. Seven voltage levels include each DC bus voltage, their sum and subtraction. Switching pattern is designed based on the redundant switching states and multicarrier level-shifted pulse width modulation (PWM) technique to help controlling the capacitor voltage at the desired level. Simulation results are presented to validate the effective voltage balancing procedure integrated into switching technique and consequently generating the 7-level voltage waveform at the output with low harmonic contents.**

***Index Terms*—multilevel inverter, cascaded H-bridge, multicarrier PWM, single DC source, power quality.**

I. Introduction

Power quality has been a major issue since using nonlinear loads in power systems. Active and passive filters have been introduced many years back to reduce the voltage/current harmonics in electricity networks and consequently to enhance the power quality. Active converters with the help of developed semiconductor switches play an important role in eliminating the undesired harmonics from system voltage/current waveform [1-4]. However, it becomes a crucial concern when the operating condition goes to high power applications in range of kilowatts and megawatts. Two-level converters known as full bridge or 6-switch cannot generate a high quality waveform without bulky passive filters at the output. Moreover, in high power applications, switching frequency and voltage ratings of the semiconductor devices limits the use of existing conventional converters [5, 6].

Multilevel inverter is a fresh emerging technology that owns both features including low harmonic waveform generation and useable in high power applications. Multilevel converters produce numerous voltage levels at the output due to having more than one DC sources and various switching paths. Different voltage levels form a multilevel waveform which is quasi-sine wave and contains less harmonics than the two-level square waveforms generated by conventional converters. Eliminating voltage harmonics just by generating multilevel waveform helps reducing the filter size at the output of the inverter. On the other hand, dividing the voltage stress between various switches makes it operational in high power applications while in conventional inverters, two switches are conducting at every switching cycle with high voltage rating [7, 8].

Various multilevel inverter topologies have been proposed including neutral point clamped (NPC) and cascaded H-bridge (CHB) as the most famous ones. NPC features common DC bus for 3-phase configuration and CHB benefits from modular structure interesting for industries [9, 10]. The main drawback of multilevel inverters is using more than one isolated DC source that each one means a transformer and a rectifier to the industry. Most of the introduced multilevel topologies require more than one isolated DC supply which makes them bulky and expensive to implement [11-18]. As a remedy to that issue, some interesting topologies have been designed using only a single DC source while replacing other DC links with capacitors as energy storage components. In such multilevel inverters, capacitors voltages are regulated at desired values to generate various voltage levels at the output. A voltage controller is a main part of these configurations [19-24]. In this regard, single DC source CHB multilevel inverter has been reported in the literature [25] and implemented with different switching technique such as selective harmonic elimination and phase-shift PWM [26-30]. The main defect of this configuration is its dependency to modulation index and load impedance to regulate the capacitor voltage well. It is notable that this scheme does not work on high modulation index [31].

In this paper, the single DC source CHB inverter is implemented using a level-shifted PWM with six carrier waves to modulate the reference voltage waveform. The capacitor voltage is regulated at the half of the DC source amplitude to generate a 7-level waveform at the output. The principle advantages of multicarrier level-shifted PWM are the simplicity in hardware implementation and using arbitrary switching frequency. Each modulation level and switching state is investigated to explore the capacitor charging or discharging performance. The voltage regulator is then combined into the switching technique getting feedbacks from DC bus voltages. The single DC source CHB inverter configuration is studied in section II. Section III includes the switching design process. Eventually, simulations are performed in Matlab/Simulink and results are discussed in section IV to validate effective voltage balancing combined with the multicarrier level-shifted modulation technique.

II. Single DC Source Cascaded H-Bridge Inverter

A single DC source CHB inverter is shown in Fig. 1. The upper cell is connected to a DC supply and the lower cell is fed from a capacitor as energy storage element. The DC supply is responsible for charging the capacitor at a desired level. On the other hand, the capacitor is discharged when it is connected to the load to generate some specific voltage levels. In this case, the capacitor voltage should be regulated at half of the DC source amplitude to have a 7-level voltage waveform at the output of the inverter. To clarify, assume that the DC source voltage is 2E so the capacitor voltage would be controlled at E. consequently, the output waveform contains the voltage levels of 0, ±E, ±2E and ±3E [25]. The main point is using all the possible combinations of DC source and capacitor as two DC links. As it is clear from the figure and switching states listed in table I, the output voltage levels consist of the DC source voltage, summation of DC source and capacitor voltages as well as their subtraction. It should be noted that each pair of switches in each leg is working in complementary situation. It means that, if the upper switch is ON, then the lower one is OFF and vice versa.

Regarding Fig. 1, the output voltage waveform is related to each cell voltage as the following:

$$V_{an} = V_1 + V_2 \tag{1}$$

Where V_{an} is the output or load voltage, V_1 and V_2 are the two cells voltages, respectively.

The switch model of that inverter can be derived using the following switching function:

$$S_i = \begin{cases} 0 & if\ S_i\ is\ Off \\ 1 & if\ S_i\ is\ On \end{cases},\ i = 1,\ 2,\ 3,\ 4,\ 5,\ 6,\ 7,\ 8 \tag{2}$$

Moreover, for the complementary switches, it can be written that:

$$\begin{cases} S_2 = \overline{S_1} = 1 - S_1 \\ S_4 = \overline{S_3} = 1 - S_3 \\ S_6 = \overline{S_5} = 1 - S_5 \\ S_8 = \overline{S_7} = 1 - S_7 \end{cases} \tag{3}$$

Each cell voltage can be formulated based on the switching function as defined by Eq. (2). Therefore, the following relations are obtained:

$$\begin{cases} V_1 = S_1 V_{dc} - S_3 V_{dc} = (S_1 - S_3) V_{dc} \\ V_2 = S_5 V_C - S_7 V_C = (S_5 - S_7) V_C \end{cases} \tag{4}$$

Considering the fact that capacitor voltage is regulated at half of the DC source amplitude ($V_C = V_{dc} / 2$), Van can be formulated by substituting Eq. (4) into Eq. (2).

$$V_{an} = \left(S_1 - S_3 + \frac{S_5}{2} - \frac{S_7}{2} \right) V_{dc} \tag{5}$$

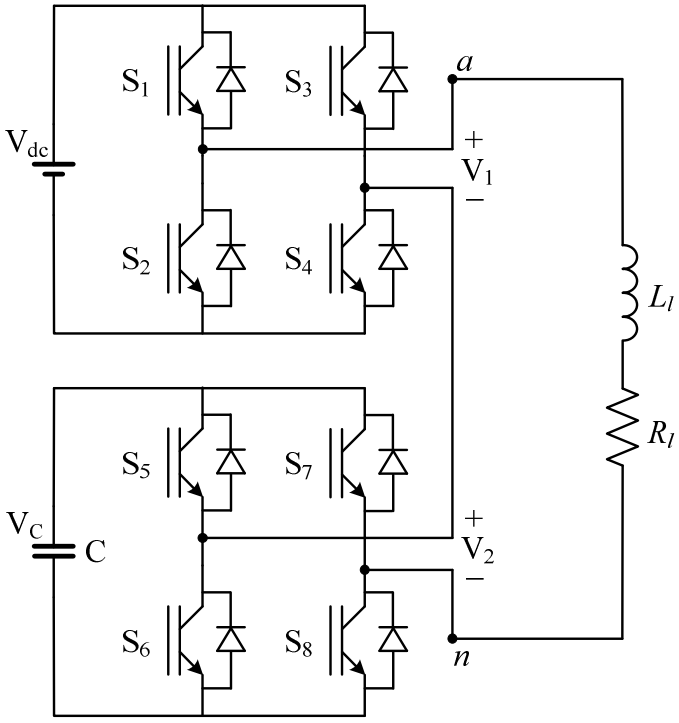

Fig. 1. Single-phase single-DC-source CHB inverter

TABLE I
SWITCHING STATES OF A SINGLE-DC-SOURCE 7-LEVEL CHB INVERTER

Switching State	S_1	S_3	S_5	S_7	V_1	V_2	V_{an}
1	1	0	1	0	$+V_{dc}$	$+V_C$	+3E
2	1	0	1	1	$+V_{dc}$	0	+2E
3	1	0	0	1	$+V_{dc}$	$-V_C$	+E
4	1	1	1	0	0	$+V_C$	+E
5	1	1	1	1	0	0	0
6	0	0	0	1	0	$-V_C$	–E
7	0	1	1	0	$-V_{dc}$	$+V_C$	–E
8	0	1	0	0	$-V_{dc}$	0	–2E
9	0	1	0	1	$-V_{dc}$	$-V_C$	–3E

Redundant switching states are obvious in table I. since the voltage regulation based on those redundancies are considered in this paper, other switching states useful for switching frequency optimization are not shown anymore. Switching states 3&4 or 6&7 are important keys to balance the capacitor voltage due to interesting charging and discharging effect. Each switching state effect is investigated in next section to use them properly in the modulation technique to produce the appropriate pulses to be sent to switches gates [32].

III. Capacitor Voltage Balancing with Multicarrier Level-Shifted PWM

Designing switching pattern in accordance with voltage balancing requires a detailed investigation of switching states influence on capacitor voltage. Therefore, every switching state is illustrated by equivalent circuit in Fig. 2. Those circuits have been drawn based on the conducting paths made by switching pulses.

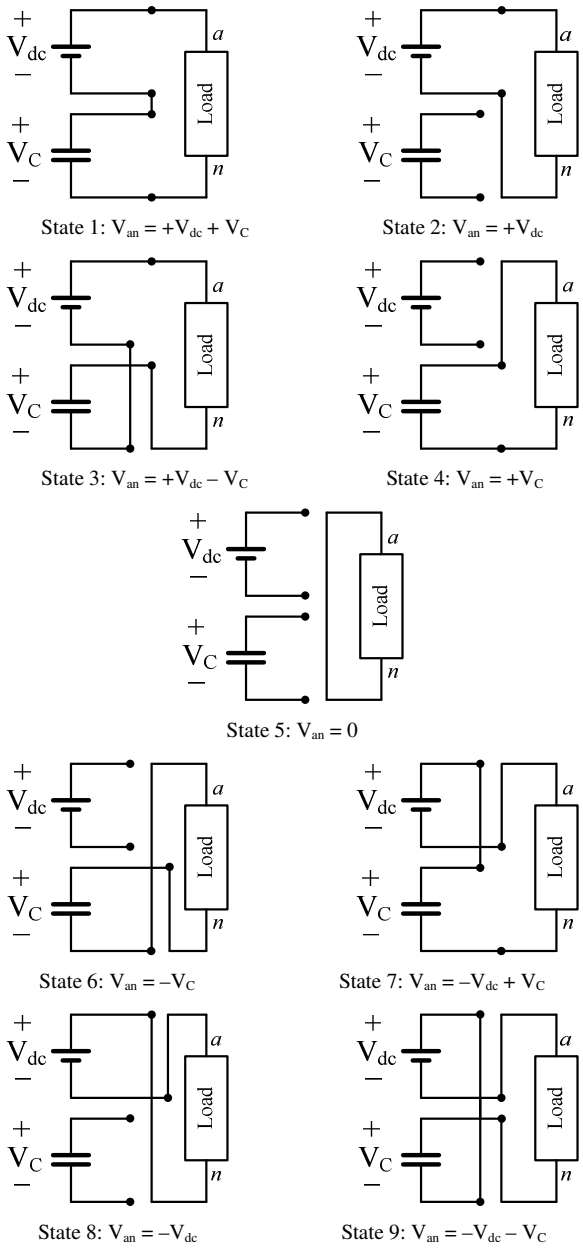

Fig. 2. Equivalent circuits of switching states listed in table I.

Analysing circuits in Fig. 2, it is clear that states 2, 5 and 8 do not affect the capacitor voltage since it is disconnected from other points. States 1 and 9 add both DC links voltages which is dependant to the capacitor time constant. In these states, the capacitor current is reversed so they are discharged quickly and then charged with reversed polarity which is undesired. A large capacitor can keep energy for a longer time so the discharging period takes more time. The longer discharging time allows the capacitor voltage to be constant at those states since they will be charged at the next coming states. Switching sequences of 3, 4, 6 and 7 affects the capacitor voltage significantly. It is clear that states 4 and 6 discharge the capacitor energy where it is connected directly to the load. On the other hand, switching cases 3 and 7 charge the capacitor voltage since it is connected to DC source in a proper direction.

TABLE II
SWITCHING EFFECTS ON CAPACITOR CHARGING AND DISCHARGING MODES

Switching State	V_1	V_2	V_{an}	Effect on Capacitor (C)
1	$+V_{dc}$	$+V_C$	+3E	Discharging
2	$+V_{dc}$	0	+2E	No Effect
3	$+V_{dc}$	$-V_C$	+E	Charging
4	0	$+V_C$	+E	Discharging
5	0	0	0	No Effect
6	0	$-V_C$	–E	Discharging
7	$-V_{dc}$	$+V_C$	–E	Charging
8	$-V_{dc}$	0	–2E	No Effect
9	$-V_{dc}$	$-V_C$	–3E	Discharging

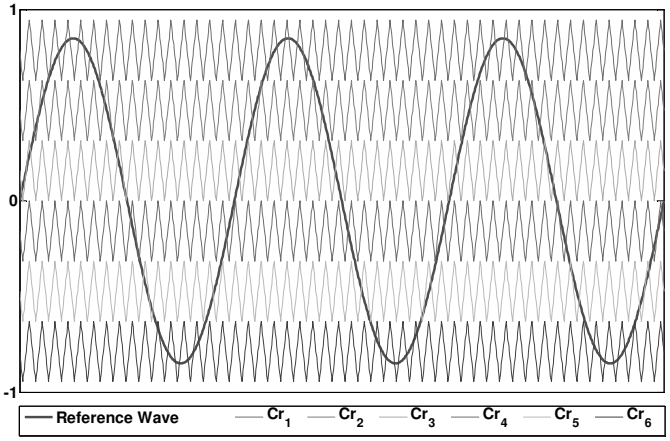

Fig. 3. Multicarrier level-shifted PWM technique

Based on the switching analysis, capacitor charge and discharge effects can be summarized in table II.

Redundant switching states include cases 3, 4, 6 and 7. Producing those states, the same voltage level is generated at the output (+E or –E) while using different switches and conduction paths. The other important point is the highest voltage level (+3E or –3E) which can discharge the capacitor and then charge it with a reversed polarity as discussed earlier. Therefore the modulation index should be low enough to prevent any long time switching on the highest level as well as being high enough to get modulated by all carrier waves as shown in Fig. 3. Missing one carrier wave, results in losing one voltage level which imposes undesired harmonics and asymmetry of the output voltage waveform.

As shown in Fig. 3, six carrier waves modulate the reference signal (V_{ref}) to generate a 7-level voltage waveform at the output of the inverter. In a two-level PWM, only one carrier wave is used (V_{cr}) with amplitude of +1 and –1. Therefore the modulation index can be defined as:

$$m_a = \frac{V_{ref}}{V_{cr}} \tag{6}$$

Based on the above relation, the modulation index can be between 0 and 1 normally however it can be greater than 1 in over-modulation area. Since numerous carrier waves are vertically shifted in multicarrier level-shifted PWM, the

maximum value is still 1 so the modulation index would be equal to the amplitude of the reference waveform ($m_a = V_{ref}$). The relation between modulation index and capacitor voltage balancing ability has been investigate in literature where a low switching frequency modulation technique was used. [31]. The same analysis for the proposed multicarrier level-shifted PWM would be done in future work to propose a solution in calculating the proper modulation index.

According to table II and Fig. 3, each switching state would be produced based on comparison between the reference signal and carrier waves. For instance, if the reference waveform (the sine wave) is greater than the highest carrier (Cr_1), then switching pulses associated with state 1 should be sent to the switches to produce the +3E voltage level at the output. To involve the redundancy states in switching process and capacitor voltage balancing, DC link voltages are sensed and used in the modulation technique accordingly. As an example, if part of a sine wave is between Cr_2 and Cr_3, the output voltage should be +E which means either state 3 or state 4 should be produced. Based on the real-time information received from voltage feedbacks, the proper switching state is selected to charge or discharge the capacitor voltage. Whole switching technique including the integrated voltage balancing method is illustrated in Fig. 4.

The proposed scheme ensures the capacitor voltage regulation at the half of DC source amplitude. The presented modulation technique is easy to implement on microcontrollers with some simple codes. Thus, it would be interesting for industries to benefit from single DC source CHB inverter in vast range of applications such as photovoltaic systems, motor drive, grid-connected inverters, electric vehicles, etc. the switching frequency can be chosen from hundred hertz to kilohertz. The only drawback of such multilevel topologies is using more voltage sensors than the conventional inverters which is necessary to control and regulate the capacitor voltage as dependent voltage source.

IV. Simulation Results and Discussion

The single DC source 7-level CHB inverter running by the designed switching pattern has been simulated in Matlab/SimPowerSystem. Results are illustrated and discussed in this section to show the effectiveness of the proposed switching technique and voltage balancing method in regulating the capacitor voltage and generating 7-level voltage waveform at the inverter output. Simulations have been performed in FixedStepDiscrete domain. Sampling time was set at 20μs. All system parameters have been listed in table III.

TABLE III
SIMULATION PARAMETERS

DC Source Votlage (V_{dc})	200 V
DC Capacitor	2.5 mF
Switching Frequency	2 kHz
Load Resistor (R_l)	40 Ω
Load Inductor (L_l)	20 mH
Load Voltage Frequency	60 Hz
Modulation Index (m_a)	0.8

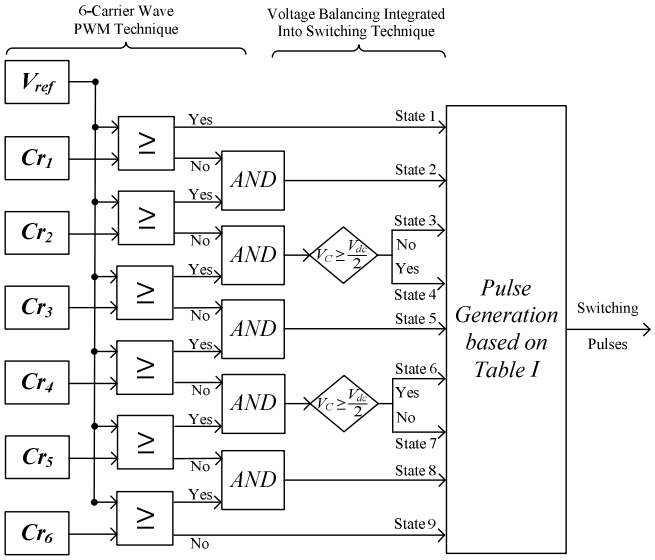

Fig. 4. Multicarrier PWM scheme with the voltage balancing procedure

In first test, the start-up condition has been examined. Therefore, the simulation has been started while the CHB inverter was connected to the load and capacitor initial voltage was zero. Fig. 5 shows the result until the system reached the steady state. Since the DC source amplitude was 200V, the capacitor voltage has been regulated at 100V successfully. The capacitor voltage ripple is less than 5% and it is acceptable practically.

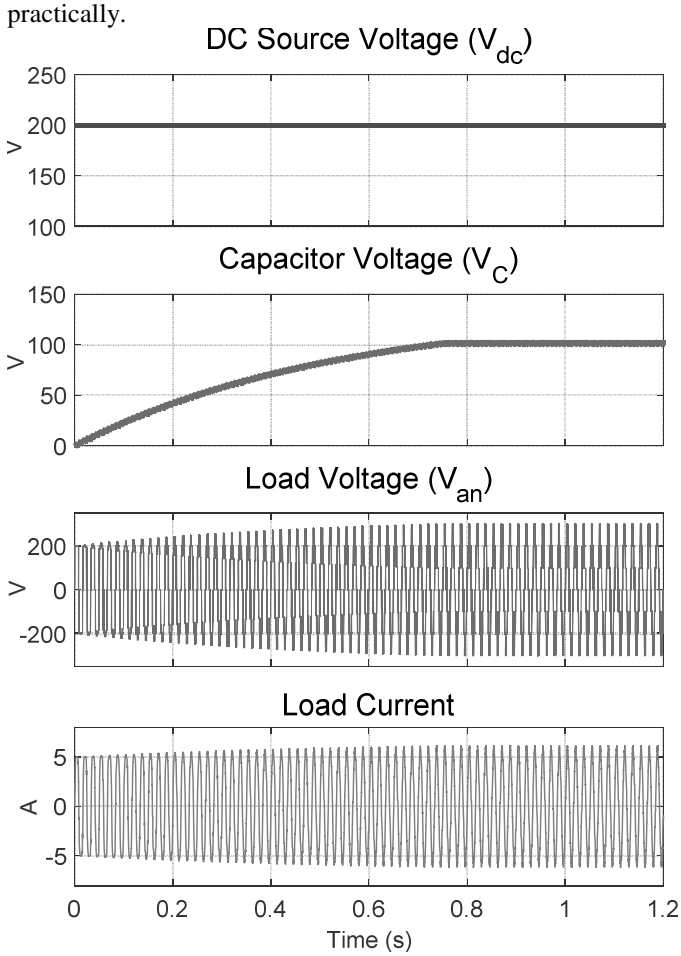

Fig. 5. Capacitor charge-up condition until reaches the steady state at 0.8s.

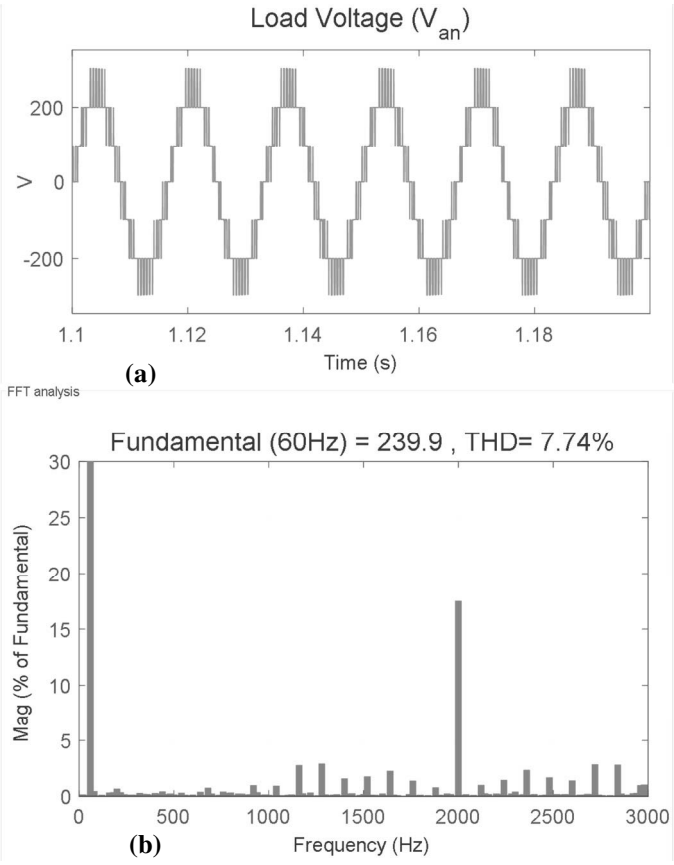

Fig. 6. Steady state 7-level voltage waveform and its FFT analysis.

After charging the capacitor, the 7-level voltage waveform is generated symmetrically as shown in Fig. 6-a. The FFT analysis of the 7-level voltage waveform has been illustrated in Fig. 6-b that proves the low harmonic content of the multilevel quasi-sine wave generated by such inverters topologies without using any additional filters at the output. The dominant harmonic order is at the switching frequency equal to the carrier waves frequencies (2000 Hz).

In continue the DC source amplitude has been changed from 200V to 300V to test the dynamic performance of the voltage balancing technique. Depicted in Fig. 7, the capacitor voltage precisely tracks the reference value which is half of the DC source magnitude. Consequently, all voltage levels are boosted and the new levels include 0, ±150V, ±300V and ±450V.

Eventually, a change in the load has been made to show the good dynamic performance of the inverter. Therefore, a nonlinear load has been added to the existing RL load. The nonlinear load has been simulated using a diode bridge rectifier connected to the resistor and inductor at its DC side. The DC resistor and inductor values have been chosen as 40Ω and 40mH that inject a vast range of harmonic into the system current. Results are shown in Fig. 8 that demonstrate no significant effect on the capacitor voltage. Due to adding parallel load, the flown current is increased which makes more ripple in the capacitor voltage however it is still controlled at 100V with acceptable voltage ripple. The load current contains significant harmonics as seen in lowest part of that figure. 7-level waveform has been generated perfectly due to proper voltage balancing of the capacitor.

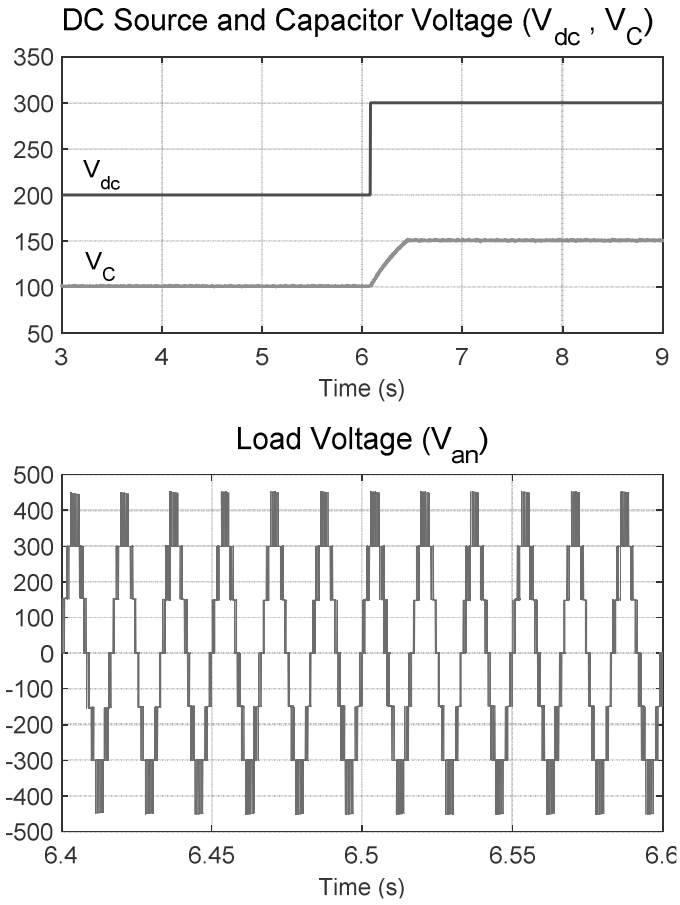

Fig. 7. Results during a 50% increase in DC source voltage from 200V to 300V

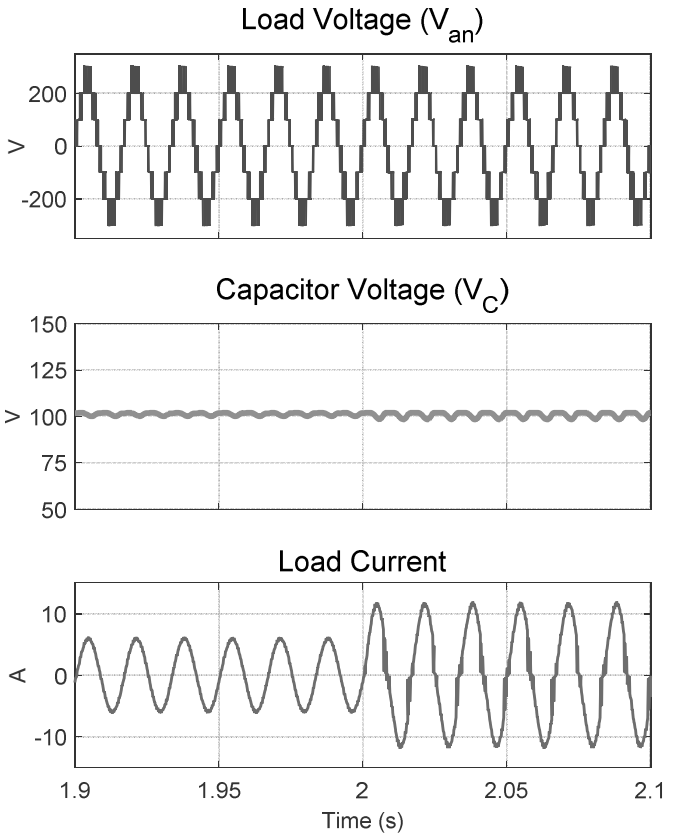

Fig. 8. Results when a rectifier as nonlinear load has been added in parallel.

V. Conclusion

In this paper 7-level CHB inverter has been investigated to use only one single isolated DC source and one capacitor as DC links. The charging and discharging paths of the capacitor have been analyzed in details. The multicarrier level-shifted PWM technique has been adopted to integrate the voltage balancing procedure using redundant switching states. The main advantage of this technique is its simplicity in hardware implementation using microcontrollers. The presented idea has been simulated and results validated the good dynamic performance of the voltage balancing process integrated into the switching technique. Different transient including change in DC source amplitude and load variations have been applied on the running inverter and the capacitor voltage tracked the reference value acceptably. The main defect of this scheme is the limited modulation index which will be investigated and discussed in future work.

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