Improved Application of Surge Capacitors for TRV Reduction When Clearing Capacitor Bank Faults

Pratap G. Mysore, *Senior Member, IEEE*, Bruce A. Mork, *Senior Member, IEEE*, and Himanshu J. Bahirat, *Student Member, IEEE*

***Abstract*—Current-limiting reactors are placed in series with capacitor banks to limit the rate of rise of current to the values specified in the circuit breaker (CB) standards. But this arrangement has created capacitor bank failures when attempting to clear faults in between the reactor and the capacitor bank. After detailed analyses of failures, solutions have been proposed by researchers: 1) Add a surge capacitor to ground on the capacitor bank side of the breaker and 2) add a surge capacitor across the reactor. These surge capacitors are sized based on the stray capacitances of the bus, the reactor, the circuit breaker, and on the maximum-available fault current at the substation. This paper presents a simplified means of sizing the surge capacitors for method 2), based only on the CB's interrupting current rating and reactor size. This eliminates the need for and uncertainty of stray capacitance values. Also, the design does not need to be revisited when grid enhancements increase the available fault current at a substation. A standard surge protection package, which can also be applied to existing installations, is proposed. This new approach has been verified with studies using Electromagnetic Transients Program/Alternative Transients Program.**

***Index Terms*—Current limiting reactor, inrush currents, outrush currents, transient recovery voltage.**

I. Introduction

CURRENT-LIMITING reactors (CLRs) are installed by utilities on capacitor banks to limit inrush, back-back energization, and outrush transients. The CLRs are sized in order to limit the peak transient current times frequency product $I_p \times f$ to the limits specified in C37.06-2000 [4], [8]. The CLR size increases with the MVAr size and with the number of paralleled-switched capacitor banks. The CLR, however, results in a high rate of rise of recovery voltage (RRRV) on the CLR side of the circuit breaker (CB) when interrupting faults [1]. NERC recently issued an industry advisory, pointing out the consequences of the high RRRV caused by the reactor-limited fault [2], [3]. A CB had failed to interrupt fault on the capacitor bank due to high RRRV.

Manuscript received April 15, 2009; revised February 27, 2010. Date of publication August 23, 2010; date of current version September 22, 2010. This work was supported by Xcel Energy, Inc., Minneapolis, MN. Paper no. TPWRD-00874-2008.

P. G. Mysore is with Xcel Energy, Inc., Minneapolis, MN 55401 USA (e-mail: Pratap.G.Mysore@xcelenergy.com).

B. A. Mork and H. J. Bahirat are with the Department of Electrical Engineering, Michigan Technological University, Houghton, MI 49931 USA (e-mail: bamork@mtu.edu; hjbahira@mtu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPWRD.2010.2050605

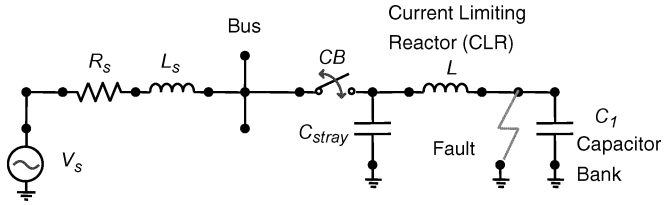

Fig. 1. Typical capacitor bank installation with the CLR.

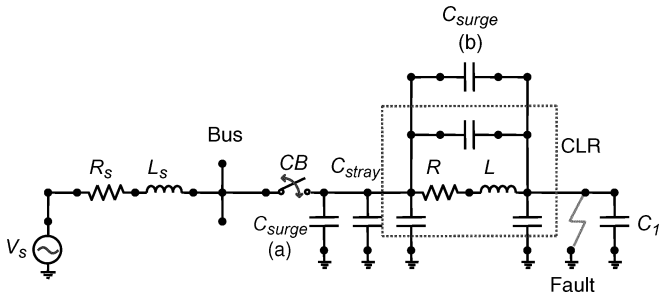

Fig. 2. Typical application of the surge capacitor can be either (a) at a circuit-breaker terminal or (b) across CLR terminals.

II. High Transient Recovery Voltage Phenomenon

Fig. 2 shows an example of a 161-kV 60-MVAR capacitor bank installation with a 300-μH CLR, and a 2000-A, 31.5-kA, 170-kV CB. A high-frequency model of the CLR is used. High RRRV problems can be mitigated either by a) adding a surge capacitor to ground on the capacitor bank side of the breaker or b) adding a surge capacitor across the CLR.

The peak voltage across the CLR during steady-state operation is only a small fraction of the bus voltage, but this value increases greatly during faults. The peak CLR voltage is given by (1) for a fault between the CLR and the capacitor bank and increases in direct proportion with the peak value of the fault current

$$V_L = I_{sc} \times \omega L \tag{1}$$

where

V_L peak CLR voltage (in kilovolts);

$I_{\rm sc}$ peak short-circuit current (in kiloamperes);

L inductance of current-limiting reactor

$$f = \frac{1}{2\pi\sqrt{LC_{\rm stray}}} \tag{2}$$

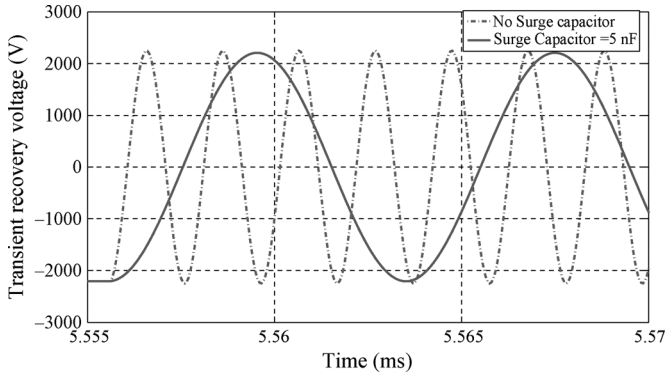

Fig. 3. Transient recovery voltage on the CLR side of the circuit breaker without a surge capacitor. Fault current $= 15$ kA CLR $= 300\ \mu$H.

f frequency of oscillation (in Hertz);

C_{stray} stray capacitance on the reactor side of the breaker.

As per (2), the peak CLR voltage upon interruption oscillates at a frequency determined by the inductance of the CLR and the stray capacitance. The high frequency of oscillation of the CLR voltage is due to low stray capacitance associated with the typical installation [1], [3]. Assuming typical capacitance values for bus, breaker bushing capacitance, and the CLR as specified in C37.011 [6], the total capacitance would be around 300–400 pF. The frequency of oscillation for the 300 μH CLR is thus in the range of 400–500 kHz.

As an example, even for a modest 15-kA [root mean sqaure (rms)] available fault current at the bus, the peak CLR voltage would be around 2.4 kV and would oscillate at around 500 kHz. The resulting RRRV is around 4.5 kV/μs which exceeds the specified 2 kV/μs in the standard. Thus, even a low level of fault current can be a major cause of failure of CBs when interrupting this type of fault.

The high RRRV can be mitigated by connecting a 5-nF surge capacitor across the CLR. Fig. 3 shows the TRV after connection of the paralleled 5-nF capacitor, which limits the RRRV to 1.1 kV/μs.

Referring again to Fig. 2, method a) could also have been used for the installation of the surge capacitor [1]. However, the installation of a surge capacitor to ground requires a more expensive capacitor rated at system voltage. Method a) also does not provide for the potential increase in the available fault current due to the expansion of the grid.

III. Proposed Approach

The proposed method is based on method 2) and has many advantages over the prevalent method 1). The proposed approach:

- eliminates the need to resize surge capacitor with an increase in available fault current;
- is based on the rated short-circuit current rating of the CB;
- allows the surge capacitors to be rated at a fraction of the system voltage values;
- is independent of the stray capacitance values;
- offers a cost-effective solution complete with protection of the surge capacitor with surge arrester;

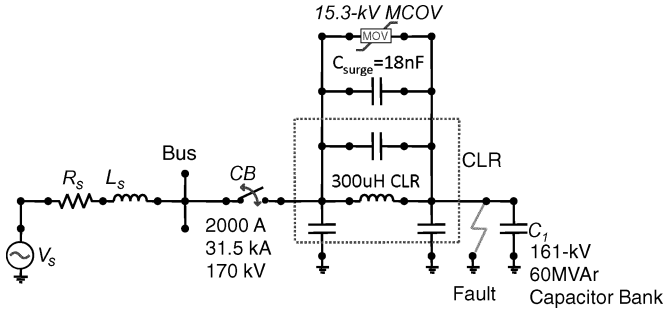

Fig. 4. Case 1 complete circuit configuration for the single bank outrush.

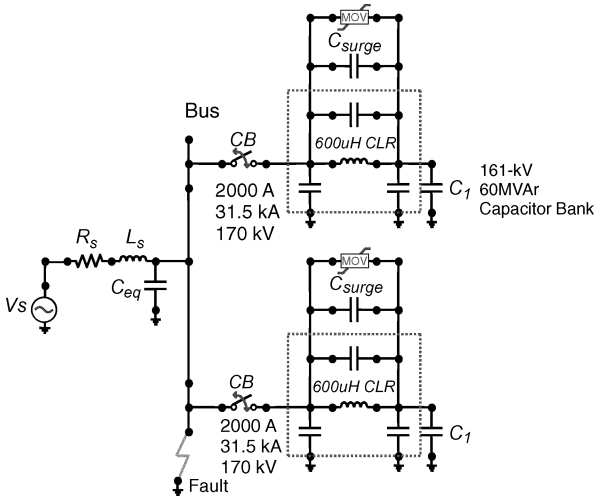

Fig. 5. Case 2 complete circuit configuration for double bank back–back energization and outrush.

- allows a standardized surge protection package design for CBs up to a 63-kA short-circuit current rating and CLR values up to 1 mH.

Two cases—Case 1 for single bank and Case 2 for double bank—shall be used to illustrate the details. The results are summarized in Figs. 4 and 5 at the end of this section.

A. CLR Sizing

Although CLRs are used to limit the rate of rise of the transient current, their size depends upon the peak system voltage level and technology of the CB (3). The CLRs are sized to limit the energization transients, but the constraining factor is typically the $I_p \times f$ capability of old oil CBs in the case of outrush. The CLR size increases in proportion to the number of parallel capacitor banks

$$I_p \times f = \frac{V_p}{2\pi L_p} \tag{3}$$

$$L_p = n \times L \tag{4}$$

V_p system peak voltage (in kilovolts);

I_p peak transient current (in amperes);

n number of parallel banks;

L_p inductance of current-limiting reactor for n capacitor banks in parallel.

The CLR value for single bank installation (Case 1) is thus 300 μH and for double bank (Case 2), it is 600 μH.

B. Sizing and Voltage Rating of Surge Capacitor

For Case 1, with a single bank and CB of the short-circuit rating of 31.5 kA (rms), the peak CLR voltage is 4.9 kV at the CB's maximum interrupting rating. The RRRV for this voltage on the CLR side of the CB is 9.8 kV/μs, which greatly exceeds the rating specified in ANSI/IEEE C37.06-2000 [4]. For correct application, the RRRV has to be reduced below 2 kV/μs. Thus, the time to reach 4.9 kV peak should be at least

$$t_1 = \left(\frac{4.9}{2}\right)\mu\text{s}. \tag{5}$$

The maximum slope of a sinusoid is at the instant of zero crossing; thus, an approximation of the maximum rate can be obtained as the time required to traverse through -30° to $+30^\circ$ (i.e., half-peak points). The allowable frequency of the TRV waveform is thus given by

$$f = \left(\frac{1}{6 \times 2.45}\right)\ \text{MHz} = 68\ \text{kHz} = \frac{1}{2\pi\sqrt{LC_{\text{surge}}}}. \tag{6}$$

Substituting (5), into (6), the minimum required value of the surge capacitor is given by

$$C_{surge} = \left(\frac{1}{L}\right) \times \left(\frac{6 \times t_1}{2\pi}\right)^2 \mu\text{F} \tag{7}$$

t_1 time to peak in microseconds;

f frequency of oscillation in Hertz;

L inducatance of current-limiting reactor μH.

The surge capacitance thus obtained is approximately 18 nF. The voltage rating of the surge capacitor should be chosen to be greater than the peak CLR voltage during the fault at the CB's fault current rating which, in this case, is 3.5 kV (rms) or 4.9 kV peak.

For the double bank of Case 2, the CLR value is 600 μH. The same procedure as used for the single bank case is used to calculate the surge capacitor value. Using (5)–(7), the required value of the surge capacitor is around 38 nF. Since the highest value of CLR for installations under consideration is 1 mH and the highest CB short-circuit rating is 63 kA, these values are used to select a surge arrester rating. A fault current of 63 kA and a 1-mH CLR will result in 23.5 kV (rms). The surge capacitor voltage rating is thus selected to be 22.8 kV which is adequate when used together with a surge arrester.

C. Need for Surge Arrester

The proposed method effectively mitigates the TRV on the CLR side of the CB. However, during close-in external faults (outrush) and back–back bank energization, high transient voltages are imposed across the CLR-surge capacitor combination. The surge capacitor is protected by connecting a low-cost distribution class surge arrester across the CLR-surge capacitor arrangement. The surge arrester rating is selected in order to limit the transient voltage to twice the surge capacitor voltage rating.

During outrush and back–back bank energization, the first peak of the voltage across the surge capacitor-CLR arrangement is given by (8). The capacitor bank capacitance is the dominating effect in the frequency of oscillation. A peak voltage up to 131 kV can appear on the surge capacitor

$$V_{\text{peak}} = \frac{EC_1}{C_1 + C_{\text{surge}}} \tag{8}$$

V_{peak} first peak voltage imposed on the surge capacitance and CLR combination (in kilovolts);

E system-phase peak voltage (in kilovolts);

L inducatance of current-limiting reactor (in microHenries);

C_1 capacitor bank capacitance (in microfarads);

C_{surge} surge capacitance (in μF).

A 15.3-kV distribution class surge arrester is selected to limit the transient voltage to 2 p.u. based on the surge capacitor voltage rating of 22.8 kV. The proposed arrangement, complete with the protection for the surge capacitor for the case of a single capacitor bank (Case 1), is shown in Fig. 4.

For Case 2, the proposed arrangement is shown in Fig. 5 with a CLR value of 600 μH with a surge capacitor of 38 nF. The rating of the surge arrester is selected to be 15.3 kV as the voltage imposed across the combination will remain unchanged with the addition of capacitor banks in parallel.

The proposed installation can be extended for the n-parallel banks, with the same selected rating of the surge arrester as for the single bank case. The surge capacitor has to be calculated for the CLR size pertaining to n-parallel banks. The maximum voltage appearing across the CLR-surge capacitor combination of the nth bank, for outrush and back-back energization, is the system voltage.

D. Restrike Conditions and Surge Arrester Sizing

The surge arrester is selected to limit the CLR-surge capacitor voltage to within 2 p.u of the surge capacitor rating. A high magnitude restrike current will result in high voltage across the CLR-surge capacitor combination. The CB restrike occurs about one-half cycle after de-energization of a capacitor bank [10]. The very high recovery voltage due to the stored charge on the capacitor bank causes a CB restrike. The surge arrester is likely to be subjected to a severe energy duty during restrike conditions and needs to be capable of handling the energy dissipated due to restrike. The recovery voltage and the resulting restrike current increases as the CB restrikes multiple times. Thus, multiple restrikes will impose extreme energy duty on surge arresters. The proposed arrangement of Fig. 4 is subjected to a single restrike to evaluate the suitability of surge arrester applications. Multiple restrikes are not considered here, as explained in the results section.

IV. Simulation

EMTP simulations were set up and run to verify the proposed scheme and to determine a standard rating for the surge capacitor and the surge arresters for fault currents up to 63 kA and

TABLE I
RECOVERY VOLTAGE, FAULT CURRENT, RISE TIME, AND RRRV FOR TRV ANALYSIS

Current Limiting Reactor (CLR)	Fault current	Surge Capacitor														
		0nF			5nF			18nF			45 nF			250nF		
		Reactor Side			Reactor Side			Reactor Side			Reactor Side			Reactor Side		
		Recovery Voltage Peak	Rise time	RRRV	Recovery Voltage Peak	Rise time	RRRV	Recovery Voltage Peak	Rise time	RRRV	Recovery Voltage Peak	Rise time	RRRV	Recovery Voltage Peak	Rise time	RRRV
		kV	μs	$kV/\mu s$	kV	μs	$kV/\mu s$	kV	μs	$kV/\mu s$	kV	μs	$kV/\mu s$	kV	μs	$kV/\mu s$
$300\mu H$	10kA	3.19	1.00	3.19	3.16	4.00	0.79	3.16	7.30	0.43	3.16	11.60	0.27	3.16	27.10	0.12
	15kA	4.45	1.00	4.45	4.41	4.00	1.10	4.41	7.30	0.60	4.41	11.60	0.38	4.41	27.10	0.16
	31.5kA	9.79	1.00	9.79	9.71	4.00	2.43	9.71	7.30	1.33	9.71	11.60	0.84	9.70	27.10	0.36
	40kA	12.31	1.00	12.31	12.21	4.00	3.05	12.20	7.30	1.67	12.20	11.60	1.05	12.20	27.10	0.45
	63kA	19.10	1.00	19.10	18.94	4.00	4.74	18.94	7.30	2.59	18.93	11.60	1.63	18.93	27.10	0.70
$500\mu H$	10kA	5.26	1.30	4.04	5.23	5.10	1.03	5.23	9.50	0.55	5.23	14.90	0.35	5.23	35.00	0.15
	15kA	7.31	1.30	5.62	7.27	5.10	1.43	7.27	9.50	0.77	7.27	14.90	0.49	7.27	35.00	0.21
	31.5kA	15.79	1.30	12.15	15.79	5.10	3.10	15.79	9.50	1.66	15.79	14.90	1.06	15.79	35.00	0.45
	40kA	19.83	1.30	15.26	19.73	5.10	3.87	19.73	9.50	2.08	19.73	14.90	1.32	19.72	35.00	0.56
	63kA	30.28	1.30	23.29	30.12	5.10	5.91	30.11	9.50	3.17	30.11	14.90	2.02	30.11	35.00	0.86
$600\mu H$	10kA	6.28	1.40	4.49	6.25	5.70	1.10	6.25	10.40	0.60	6.25	16.30	0.38	6.25	38.40	0.16
	15kA	8.72	1.40	6.23	8.68	5.60	1.55	8.67	10.40	0.83	8.67	16.30	0.53	8.67	38.40	0.23
	31.5kA	18.81	1.40	13.44	18.72	5.60	3.34	18.72	10.40	1.80	18.72	16.30	1.15	18.72	38.90	0.48
	40kA	23.44	1.40	16.74	23.32	5.50	4.24	23.32	10.40	2.24	23.32	16.30	1.43	23.32	38.50	0.61
	63kA	35.51	1.40	25.36	35.33	5.60	6.31	35.33	10.40	3.40	35.32	16.30	2.17	35.32	38.90	0.91
$750\mu H$	10kA	7.80	1.60	4.87	7.77	6.30	1.23	7.77	11.60	0.67	7.77	18.30	0.42	7.77	43.00	0.18
	15kA	10.80	1.60	6.75	10.76	6.30	1.71	10.76	11.60	0.93	10.76	18.30	0.59	10.76	43.00	0.25
	31.5kA	23.08	1.60	14.42	23.00	6.30	3.65	22.99	11.60	1.98	22.99	18.30	1.26	22.99	43.00	0.53
	40kA	28.63	1.60	17.89	28.53	6.30	4.53	28.52	11.60	2.46	28.52	18.30	1.56	28.52	43.00	0.66
	63kA	42.89	1.60	26.81	42.74	6.30	6.78	42.73	11.60	3.68	42.73	18.30	2.33	42.73	43.00	0.99
$1000\mu H$	10kA	10.28	1.80	5.71	10.26	7.20	1.42	10.25	13.50	0.76	10.25	21.10	0.49	10.25	49.70	0.21
	15kA	14.19	1.80	7.88	14.19	7.20	1.97	14.15	13.50	1.05	14.15	21.10	0.67	14.15	49.70	0.28
	31.5kA	29.87	1.80	16.59	29.79	7.20	4.14	29.79	13.50	2.21	29.78	21.10	1.41	29.78	49.70	0.60
	40kA	36.80	1.80	20.45	36.70	7.20	5.10	36.70	13.50	2.72	36.70	21.10	1.74	36.70	49.70	0.74
	63kA	54.19	1.80	30.11	54.04	7.20	7.51	54.03	13.50	4.00	54.03	21.10	2.56	54.03	49.70	1.09

TABLE II
VOLTAGE, ENERGY DISSIPATED, AND TRANSIENT FREQUENCY FOR OUTRUSH SIMULATION

Current Limiting Reactor	Fault current	Surge Capacitor											
		5nF			18nF			45nF			250nF		
		Voltage	Frequency	Energy	Voltage	Frequency	Energy	Voltage	Frequency	Energy	Voltage	Frequency	Energy
		kV	Hz	kJ	kV	Hz	kJ	kV	Hz	kJ	kV	Hz	kJ
$300\mu H$	10kA	49.37	5263.16	34.96	49.29	5263.16	34.76	49.13	5263.16	34.37	49.31	5000.00	31.59
	15kA	49.37	5263.16	34.72	49.36	5263.16	34.53	49.20	5263.16	34.14	49.38	5000.00	31.37
	31.5kA	49.28	5263.16	34.39	49.20	5263.16	34.21	49.03	5263.16	33.82	49.21	5000.00	31.06
	40kA	49.26	5263.16	34.34	49.18	5263.16	34.15	49.01	5263.16	33.77	49.19	5000.00	31.01
	63kA	49.23	5263.16	35.26	49.15	5263.16	34.08	48.99	5263.16	33.69	49.17	5000.00	30.94
$600\mu H$	10kA	49.50	3703.70	35.11	49.42	3703.70	34.92	49.25	3703.70	34.52	49.43	3571.43	30.71
	15kA	49.36	3703.70	34.72	49.35	3703.70	34.68	49.18	3703.70	34.29	49.36	3571.43	31.49
	31.5kA	49.33	3703.70	34.55	49.25	3703.70	34.36	49.09	3703.70	33.97	49.26	3571.43	31.18
	40kA	49.31	3703.70	34.49	49.23	3703.70	34.30	49.07	3703.70	33.91	49.24	3571.43	31.13
	63kA	49.29	3703.70	34.42	49.21	3703.70	34.23	49.05	3703.70	33.84	49.36	3571.43	31.06

TABLE III
VOLTAGE, ENERGY DISSIPATED, AND TRANSIENT FREQUENCY FOR BACK–BACK ENERGIZATION

Current Limiting Reactor		Fault current	Surge Capacitor							
			5nF		18nF		45nF		250nF	
			Voltage	Energy	Voltage	Energy	Voltage	Energy	Voltage	Energy
			kV	kJ	kV	kJ	kV	kJ	kV	kJ
$600\mu H$	$1^{st} Bank$	10kA	50.20	4.76	50.13	4.71	49.97	4.62	48.74	4.03
		15kA	50.07	4.68	50.06	4.68	49.90	4.59	48.66	4.01
		31.5kA	50.03	4.71	49.95	4.68	49.80	4.57	48.56	4.03
		40kA	50.01	4.72	49.94	4.68	49.78	4.58	48.54	4.07
		63kA	49.99	4.77	49.91	4.72	49.75	4.63	48.51	4.23
	$2^{nd} Bank$	10kA	49.37	4.75	50.13	4.70	49.97	4.61	48.74	4.00
		15kA	49.37	4.67	50.06	4.66	49.90	4.57	48.67	3.96
		31.5kA	49.28	4.68	49.97	4.63	49.80	4.53	48.57	3.90
		40kA	49.26	4.69	49.95	4.64	49.79	4.54	48.55	3.89
		63kA	49.23	4.79	49.93	4.73	49.77	4.62	48.53	3.91

CLRs sizes up to 1 mH. Tables I–III give the simulation results.

V. RESULTS AND ANALYSIS

Table I summarizes the results obtained from the TRV simulation. The sensitivity analysis of the results confirms that the CLR voltage and RRRV increase in proportion with the fault current, with the highest values being noted for a fault current of 63 kA (rms). Fig. 6 demonstrates the effective mitigation of high RRRV by comparing the TRV waveforms with and without the connection of an 18-nF surge capacitor calculated by using the proposed calculation approach.

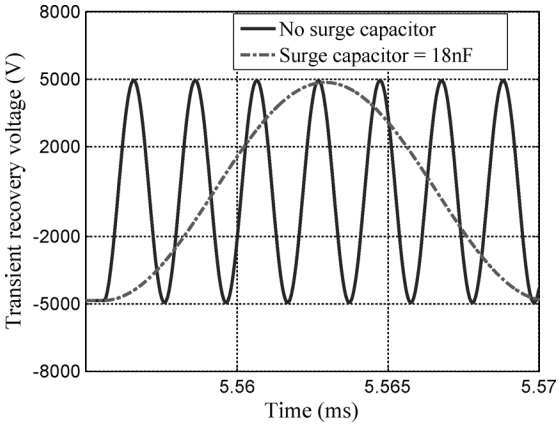

Fig. 6. Comparison of the recovery voltage with and without the surge capacitor for a fault current of 31.5 kA (rms).

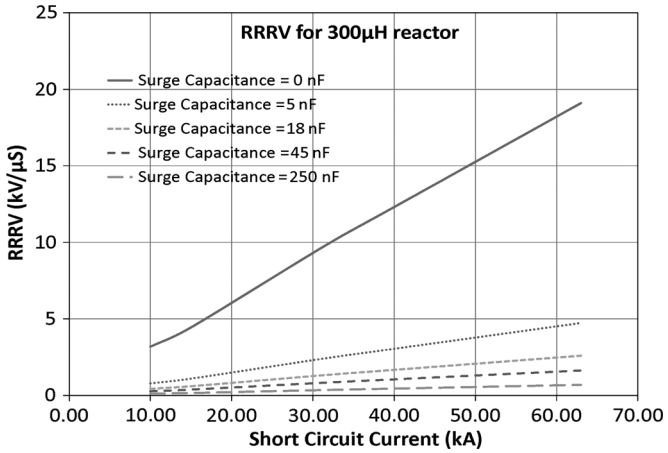

Fig. 7. Variation RRRV for a 300-μH CLR with different values of surge capacitance.

Fig. 7 shows the variation of the RRRV for 300-μH CLR for the variation of surge capacitors and the fault current values. The 18-nF surge capacitor value calculated with the proposed approach is seen to effectively limit the RRRV below 2 kV/μs for fault current up to 31.5 kA (rms), the short-circuit rating of the CB. The results in Table I validate the proposed calculation method of the surge capacitor values based on the CB short-circuit rating. Thus, the generic mitigation with the CB short-circuit rating can be used and it caters to the lesser available values of fault current. The fault current values reported in Table I correspond to bus fault currents. The peak recovery voltage is less than the fault current times the reactance because of the voltage drop across the source impedance.

Tables II and III summarize the results for sensitivity analysis for outrush transients and back–back energization, respectively. The values of CLR used for simulation are in accordance with (3) and (4), thus corresponding to a 300-μH CLR for single bank, a CLR of 600 μH was used for the back–back energization and outrush simulation studies. Fig. 8 contrasts the maximum voltage across the CLR-surge capacitor combination with and without arresters.

The sensitivity analysis also confirms that the voltage imposed across the combination is independent of the reactor

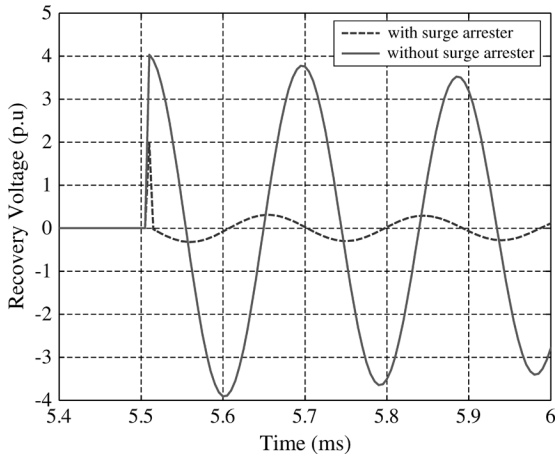

Fig. 8. Voltage across the CLR-surge capacitor combination during outrush transient with and without surge arresters protecting the surge capacitor. Fault current = 31.5 kA, surge capacitor = 18 nF.

values. The frequency of oscillation is dominated by the capacitor bank capacitance. The results confirm that the surge capacitor will be subjected to a high voltage close to the rated system voltage. The highest value measured during simulation is around 129 kV peak; thus, the protection of the surge capacitor is in order. The connection of the 15.3-kV surge arrester limits the CLR voltage to 50.2 kV peak. It can be concluded from the results that the selection of the surge arrester with the MCOV rating equal to or higher than the maximum CLR voltage can effectively limit the CLR voltage to within capabilities of the surge capacitor. The voltage poses no threat to the CLR, as their ratings are based on the system voltage rating and, thus, they have an adequate insulation level to withstand the CLR voltage.

Fig. 9 shows the energy dissipated in the surge arrester, with the highest energy dissipation occurring in phase B. This is in accordance with the observed maximum on phase B without the surge arrester. The phase B voltage is clipped to a value lower than 2 p.u. on the voltage base of the surge capacitor. The maximum energy dissipated in the 15.3-kV MCOV surge arrester is found to be 33 kJ, which is well within the limits of the surge arrester rating. The energy dissipated in the surge arresters for back–back energization is less for outrush because the voltage to which the CLR-surge capacitor combination is subjected is halved. The frequency of the transient current is not affected by the surge arrester.

This demonstrates the validity of the proposed design approach and shows the effect of variation of the parameters from the standard values. Based on the results obtained, a standardization design is proposed in the next section.

Modern power CBs have a very low probability of restrike. Standards C37.04 [5] and C37.09 [9] define two classes of CBs—Class C1 with low probability and Class C2 with a very low probability of restrike. Standard C37.09 allows for only one restrike inside a gas CB without arc shunting resistance. Oil CBs are also expected to handle only one restrike. As new installations have gas CBs, only one restrike per operation is thus considered for evaluation of this application. Fig. 10 shows energy dissipated in a 15.3-kV surge arrester connected across

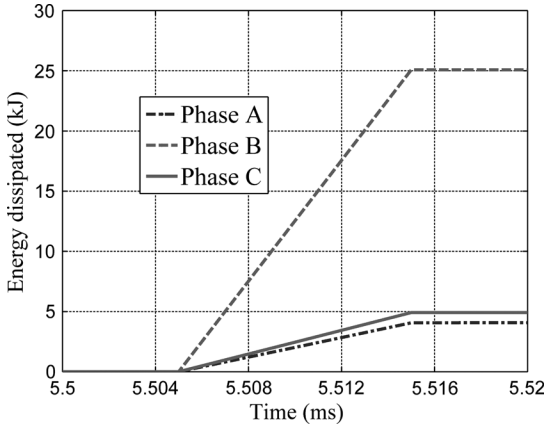

Fig. 9. Energy dissipated in the surge arrester for the 31.5-kA circuit with an 18-nF surge capacitor and a 15.3-kV MCOV arrester.

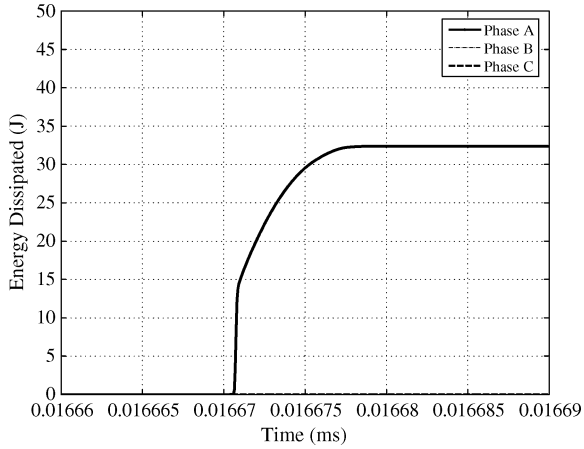

Fig. 10. Energy dissipated in a 15.3-kV MCOV surge arrester for the 31.5-kA circuit for a single restrike.

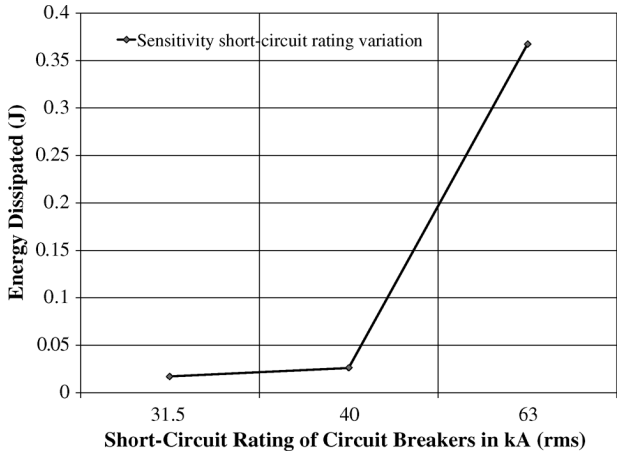

Fig. 11. Restrike: Sensitivity study for the CB short-circuit rating variation and 600-μH CLR.

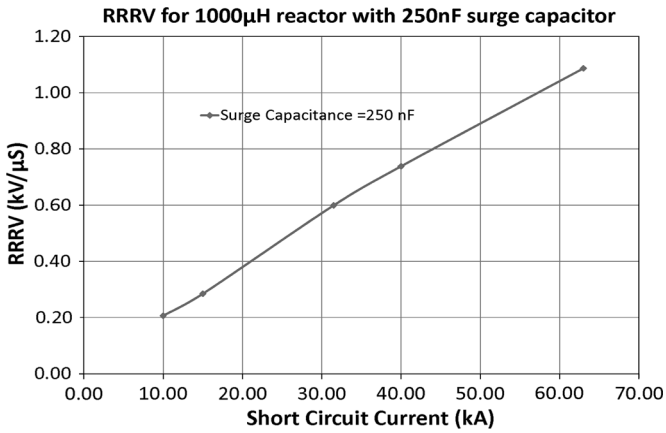

Fig. 12. Variation RRRV for a standardized installation of 1000-μH CLR and 250-nF surge capacitance.

a 600-μH CLR. The small amount of energy dissipated is well within the limits of the arrester.

Fig. 11 shows the results of sensitivity analysis performed with the variation of the CB short-circuit rating. For a given system voltage and short-circuit rating of the CB, the energy dissipated in the arrester increases with an increase in bank size. The sensitivity analysis with respect to the CB short-circuit rating (Fig. 11) shows that the energy dissipated in the arrester increases but is within limits of the arrester capability.

For the case of ungrounded capacitor banks, it was observed that the restrike current does not reach very high magnitudes; thus, the energy dissipated in the 15.3-kV surge arresters connected across 1000 μH is well within the arrester's energy capability.

VI. Standardization

The proposed scheme provides a standardized surge protection package for the installation of CLRs up to 1 mH with short-circuit ratings up to 63 kA. A 22.8-kV, 50-kVAr, 250-nF surge capacitor and surge arrester rated at 15.3-kV MCOV across the CLR can reduce the rate of rise of the recovery voltage below the breaker RRRV design limit. This standardization greatly reduces the study efforts for retrofits on existing capacitor bank installations. The suitability of the proposed standardization is verified by simulations up to the system voltage 161 kV. The sensitivity analysis results are given in Table I. Fig. 11 shows variation of RRRV for the standardized installation. The maximum RRRV is seen to be 1.09 kV/μs. which is well below the rating of 2 kV/μs. The surge arrester rating is also found to be adequate to limit the voltage across the CLR-surge capacitor combination to 2 p.u. on the voltage base of the surge capacitor.

The sensitivity analysis shows that a 15.3-kV surge arrester has adequate reserve capability to handle one restrike when connected across a 1000-μH CLR. However, the application of a single 15.3-kV arrester may not be suitable for the case of multiple restrikes, wherein the energy capability of the arrester may be exceeded. The maximum energy dissipated in an arrester connected across the 1000-μH CLR on the 161-kV 120-MVAr capacitor bank installation with the 63-kA CB is found to be 24 kJ. Fig. 13 shows the results of sensitivity analysis with respect to the CB short-circuit rating for 1000-μH CLR installation.

VII. Conclusion

The following conclusions can be drawn based on the analysis of the results.

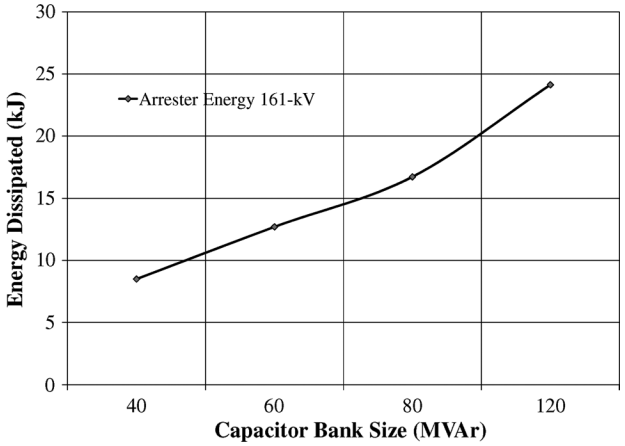

Fig. 13. Restrike: Sensitivity study capacitor bank size variation. circuit breaker rating= 63 kA and 1000-μH CLR.

- The surge protection package across the CLR provides a cost-effective solution to the industry concern on the failure of capacitor bank breakers due to high RRRV.
- The design is scalable to cases with n-parallel banks.
- The surge arrester can be rated at voltage equal to or greater than the maximum voltage across the CLR.
- A distribution class surge arrester can be used for protection of the surge capacitor.
- There can be substantial cost benefits incurred from specification of the surge capacitor at a fraction of the system voltage rating.
- This standardized solution can reduce retrofitting efforts for existing installations.
- This design approach can also be applied to the design of the surge protection package for capacitor banks at other rated voltages.
- The surge arrester has adequate energy capability to handle a restrike in the CB.
- Multiple restrikes may be of concern, but most CBs are not rated for multiple restrikes in any case.
- The calculation method presented can be used to design the surge protection package for various CLR values higher than the standardized protection package.

REFERENCES

[1] T. A. Bellei, E. H. Camm, and G. Ransom, "Current-limiting inductors used in capacitor bank applications and their impact on fault current interruption," in *Proc. IEEE Power Eng. Soc. Transm. Distrib. Conf. Expo.*, Apr. 2001, vol. 1, pp. 603–607.

[2] North America Electric Reliability Corp., "NERC industry advisory:-excessive RRRV at capacitor banks," Jan. 2008, Tech. Rep.

[3] L. Tang and L. Marti, "Richview TS capacitor bank failure-cause of failure analysis," Special Studies Transmission System Development, Hydro One Networks Inc., Sep. 2007, Tech. Rep.

[4] *American National Standard AC High-Voltage Circuit Breakers Rated on a Symmetrical Current Basis Preferred Ratings and Related Required Capabilities*, IEEE Std. C37.06-2000, 2000.

[5] *IEEE Standard Rating Structure for AC High-Voltage Circuit Breakers*, IEEE Std. C37.04-1999, 1999.

[6] *IEEE Application Guide for Transient Recovery Voltage for AC High-Voltage Circuit Breakers*, IEEE Std. C37.011-2005, 2006.

[7] D. F. Peelo, G. S. Polovick, J. H. Sawada, P. Diamanti, R. Presta, A. Sarshar, and R. Beauchemin, "Mitigation of circuit breaker transient recovery voltages associated with current-limiting reactors," *IEEE Trans. Power Del.*, vol. 11, no. 2, pp. 865–871, Apr. 1996.

[8] A. Greenwood, *Electrical Transients in Power Systems*. New York: Wiley, 1991.

[9] *IEEE Standard Test Procedure for AC High-Voltage Circuit Breakers Rated on a Symmetrical Current Basis*, Std. C37.09, 2000.

[10] "Impact of shunt capacitor banks on substation surge environment and surge arrester applications," *IEEE Trans. Power Del.*, vol. 11, no. 4, pp. 1798–1809, Oct. 1996.

Pratap G. Mysore (SM'03) received the B.E. and M.E. degrees in electrical engineering from the Indian Institute of Science, Bangalore, India.

He has been with Xcel Energy since 1987 and is currently a Consulting Engineer (in-house position) with the Substation/Transmission Engineering Group. Prior to joining Xcel Energy, he was with Brown Boveri Corp. (now ABB) and Tata Electric Companies in India. He is actively involved in the standards development work through the IEEE Power Systems Relaying Committee (PSRC).

Mr. Mysore is the Vice-Chair of the substations subcommittee, Chair of the working group revising the shunt capacitor protection guide, and a member of several working groups within the PSRC. He is a Registered Professional Engineer in the state of Minnesota. He is also a recipient of the Twin Cities "IEEE Outstanding Engineer Award" in 2000.

Bruce A. Mork (SM'08) was born in Bismarck, ND, on June 4, 1957. He received the B.S.M.E., M.S.E.E., and Ph.D. degrees in electrical engineering from North Dakota State University in 1979, 1981, and 1992, respectively.

From 1982 to 1986, he was a Design Engineer with Burns and McDonnell Engineering, Kansas City, MO, in the areas of substation design, protective relaying, and communications. He spent three years in Norway: as a Research Engineer for the Norwegian State Power Board, Oslo, from 1989 to 1990; Visiting Researcher at the Norwegian Institute of Technology, Trondheim, from 1990 to 1991; and Visiting Senior Scientist at SINTEF Energy Research, Trondheim, from 2001 to 2002. He joined the faculty of Michigan Technological University, Houghton, in 1992, where he is currently Professor of Electrical Engineering and Director of the Power & Energy Research Center.

Dr. Mork is a member of ASEE, NSPE, and Sigma Xi. He is a Registered Professional Engineer in the States of Missouri and North Dakota.

Himanshu J. Bahirat (S'06) received the B.E. degree from Visvesvaraya Regional College of Enginnering, Nagpur, India, in 2002 and is currently pursuing the M.S.E.E. and Ph.D. degrees at Michigan Technological University, MI.

He was with Schneider Electric Private Ltd. and Larsen & Toubro Ltd. at their design centers in India, working in the area of circuit-breaker design .

Mr. Bahirat is a member of Eta Kappa Nu (HKN).